Jedi 15"/17" Schematics
WhiskyLake - U/2GB VRAM

2019-01-03

REV : A00

DY : None Installed
UMA: UMA only installed
OPS: DISCRTE OPTIMUS installed

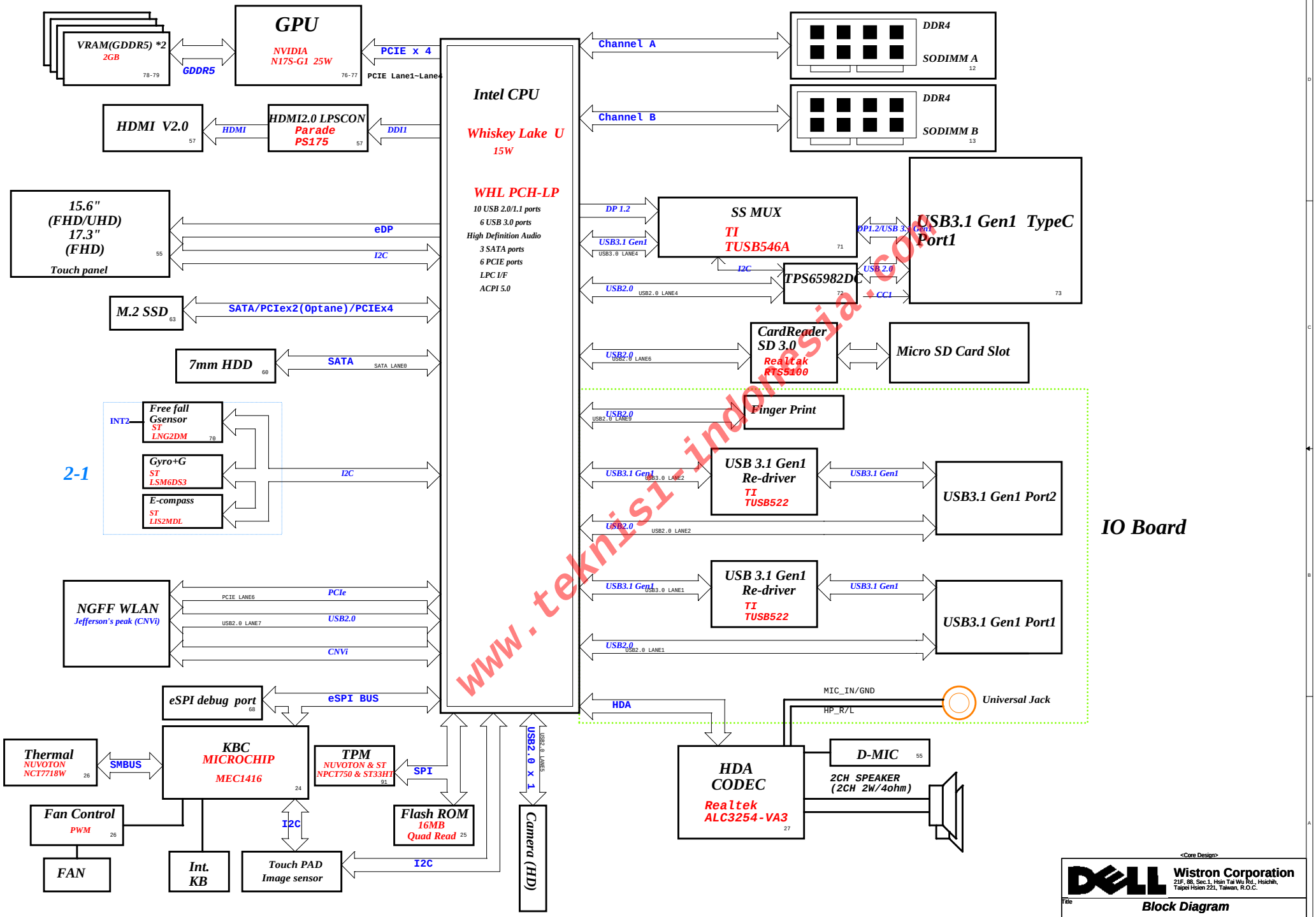
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Cover Page*		
Size: A3	Document Number: Jedi15"/17" WHL-U	Rev: A00
Date: Tuesday, January 08, 2019	Sheet 1 of 106	

Jedi 15"/17" CPU 15W + GPU 25W Block Diagram

Project code: 4PD0GE010001
PCB P/N: 18718
Revision: X02



<Core Design>

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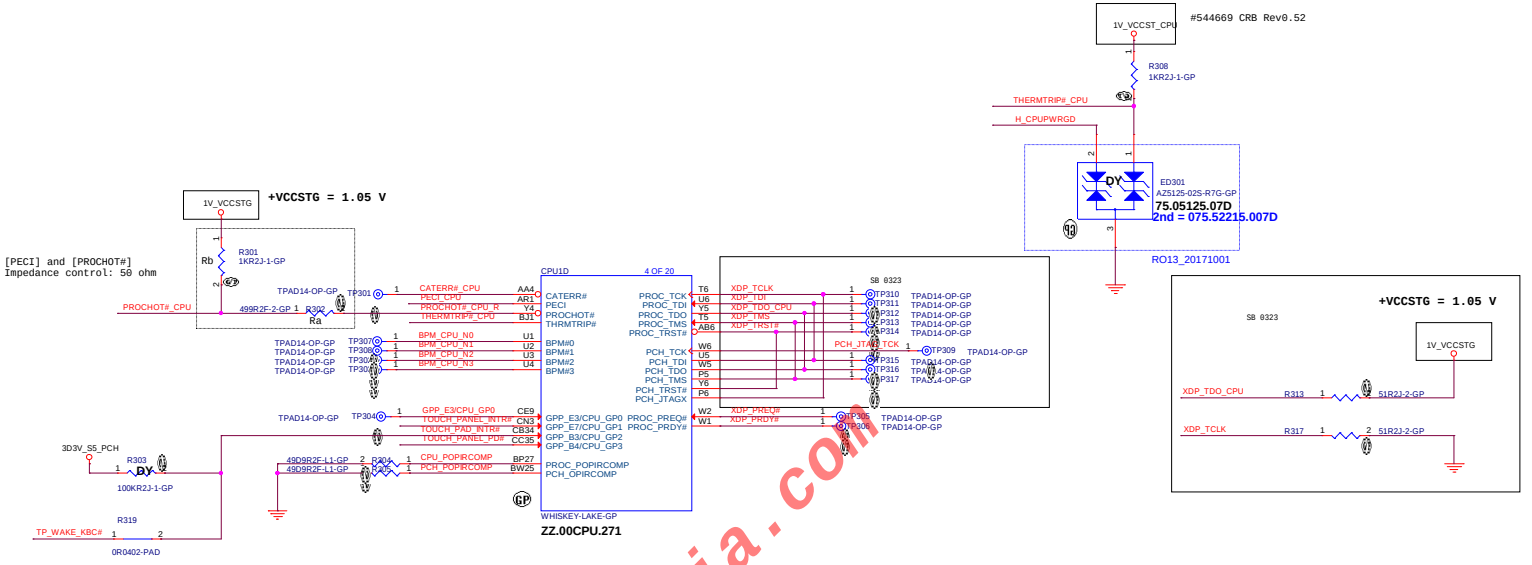
Title: Block Diagram

Size	Document Number	Rev
C	Jedi15"/17" WHL-U	A00

Date: Tuesday, January 08, 2019 Sheet 2 of 106

Main Func = CPU



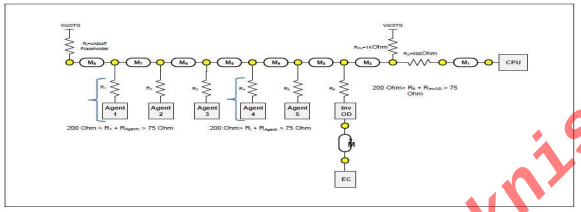


Table 7-11. PROCHOT# Routing Guidelines (Sheet 1 of 2)

Segment	Tline Type	Reference	Via Count	Max Length, mm		Max Length, Mils	
				Segment	Total	Segment	Total
M1	MS/SL/DSL	VSS	1	38	305	1496.06	12007.9
M2	MS/SL/DSL	VSS	2	279		10984.3	
M3	MS/SL/DSL	VSS	1	76		2992.13	
M4	MS/SL/DSL	VSS	1	76		2992.13	
M5	MS/SL/DSL	VSS	1	76		2992.13	
M6	MS/SL/DSL	VSS	1	76		2992.13	
M7	MS/SL/DSL	VSS	1	76		2992.13	
M8	MS/SL/DSL	VSS	1	8		341.96	
M9	MS/SL/DSL	VSS	2	254	254	10000	10000
Topology Guidelines							
Platform resistors values	Rpu=1KΩ, Rs=500Ω, Ri+Ragent=75-200Ω, R6+Rinvod=75-200Ω						
Platform resistors tolerances	± 5%						

Main Func = CPU

DP to HDMI2.0

57 HDMI_DDI_TX_N0
57 HDMI_DDI_TX_P0
57 HDMI_DDI_TX_N1
57 HDMI_DDI_TX_P1
57 HDMI_DDI_TX_N2
57 HDMI_DDI_TX_P2
57 HDMI_DDI_TX_N3
57 HDMI_DDI_TX_P3
57 DP1_AUX_CPU_N
57 DP1_AUX_CPU_P
57 HDMI_HPD_CPU

DP for Type-C Mux

71 DP2_DDI_TX_N0
71 DP2_DDI_TX_P0
71 DP2_DDI_TX_N1
71 DP2_DDI_TX_P1
71 DP2_DDI_TX_N2
71 DP2_DDI_TX_P2
71 DP2_DDI_TX_N3
71 DP2_DDI_TX_P3
71 DP2_AUX_CPU_P
71 DP2_AUX_CPU_N

55 eDP_TX_CPU_N0
55 eDP_TX_CPU_P0
55 eDP_TX_CPU_N1
55 eDP_TX_CPU_P1
55 eDP_TX_CPU_N2
55 eDP_TX_CPU_P2
55 eDP_TX_CPU_N3
55 eDP_TX_CPU_P3
55 eDP_AUX_CPU_N
55 eDP_AUX_CPU_P
55 eDP_HPD_CPU
71,72 DP1_HPD_CPU

24 L_BKLT_EN
55 L_BKLT_CTRL
55 EDP_VDD_EN

15 GPP_H17_STRAP

24 GC6_THM_DIS#

Strap pin:

Port B / Port C Detected	Sampled at rising edge of PCH_PWROK
DDPB_CTRLDATA	0 = Port B is not detected. * 1 = Port B is detected.
DDPC_CTRLDATA	0 = Port C is not detected. * 1 = Port C is detected.

These two signals have weak internal pull-down.

3D3V_S0
RN401 1 2 4 3 SRN2K2J-5-GP
CPU_DP1_CTRL_DATA
CPU_DP1_CTRL_CLK

3D3V_S0
SRN2K2J-5-GP 2 1 3 4
CPU_DP2_CTRL_DATA
CPU_DP2_CTRL_CLK
RN402

Port B **DP to HDMI2.0**

Port C **DP for Type-C Mux**

CPU1A 1 OF 20

HDMI_DDI_TX_N0	AL5	DDI1_TXN0	
HDMI_DDI_TX_P0	AL6	DDI1_TXP0	
HDMI_DDI_TX_N1	AJ5	DDI1_TXN1	
HDMI_DDI_TX_P1	AJ6	DDI1_TXP1	
HDMI_DDI_TX_N2	AF6	DDI1_TXN2	
HDMI_DDI_TX_P2	AF5	DDI1_TXP2	
HDMI_DDI_TX_N3	AE5	DDI1_TXN3	
HDMI_DDI_TX_P3	AE6	DDI1_TXP3	
DP2_DDI_TX_N0	AC4	DDI2_TXN0	
DP2_DDI_TX_P0	AC3	DDI2_TXP0	
DP2_DDI_TX_N1	AC1	DDI2_TXN1	
DP2_DDI_TX_P1	AC2	DDI2_TXP1	
DP2_DDI_TX_N2	AE4	DDI2_TXN2	
DP2_DDI_TX_P2	AE3	DDI2_TXP2	
DP2_DDI_TX_N3	AE1	DDI2_TXN3	
DP2_DDI_TX_P3	AE2	DDI2_TXP3	

		EDP_TXN0	AG4 eDP_TX_CPU_N0
		EDP_TXP0	AG3 eDP_TX_CPU_P0
		EDP_TXN1	AG2 eDP_TX_CPU_N1
		EDP_TXP1	AG1 eDP_TX_CPU_P1
		EDP_TXN2	AJ4 eDP_TX_CPU_N2
		EDP_TXP2	AJ3 eDP_TX_CPU_P2
		EDP_TXN3	AJ2 eDP_TX_CPU_N3
		EDP_TXP3	AJ1 eDP_TX_CPU_P3
		EDP_AUX_N	AH4 eDP_AUX_CPU_N
		EDP_AUX_P	AH3 eDP_AUX_CPU_P
		DISP_UTILS	AM7
		DDI1_AUX_N	AC7 DP1_AUX_CPU_N
		DDI1_AUX_P	AC6 DP1_AUX_CPU_P
		DDI2_AUX_N	AD4 DP2_AUX_CPU_N
		DDI2_AUX_P	AD3 DP2_AUX_CPU_P
		DDI3_AUX_N	AG7
		DDI3_AUX_P	AG6

SA 0131

for HDMI2.0

GPP_E13/DDPB_HPD0/DISP_MISC0	CN6	HDMI_HPD_CPU
GPP_E14/DDPC_HPD1/DISP_MISC1	CM6	DP1_HPD_CPU_R
GPP_E15/DPPD_HPD2/DISP_MISC2	CP7	SIO_EXT_SMI#
GPP_E16/DPPE_HPD3/DISP_MISC3	CP6	
GPP_E17/EDP_HPD/DISP_MISC4	CM7	eDP_HPD_CPU
EDP_BKLTEN	CK11	L_BKLT_EN
EDP_VDDEN	CG11	EDP_VDD_EN
EDP_BKLTCTL	CH11	L_BKLT_CTRL

RO13_20170626
RCOMP SHOULD BE VSS REFERNCE AND SHIELDED
CHECK WHL design guide: DISP_RCOMP
1V_VCCIO
R491 1 2 24D9R2F-L-GP
eDP_RCOMP_CPU AM6
DISP_RCOMP
CPU_DP1_CTRL_CLK CC8
CPU_DP1_CTRL_DATA CC9
CPU_DP2_CTRL_CLK CH4
CPU_DP2_CTRL_DATA CH3
GPP_E18/DPPB_CTRLCLK/CNV_BT_HOST_WAKE#
GPP_E19/DPPB_CTRLDATA
GPP_E20/DPPC_CTRLCLK
GPP_E21/DPPC_CTRLDATA
TPAD14-OP-GP TP402 1 GPP_E23 CP4 CN4
SA 0105 strap reserve
GC6_THM_DIS# CR26
GPP_H17_STRAP CP26
GPP_E22/DPPD_CTRLCLK
GPP_E23/DPPD_CTRLDATA
GPP_H16/DDPF_CTRLCLK
GPP_H17/DDPF_CTRLDATA
WHISKEY-LAKE-GP
ZZ.00CPU.271

(#543016) eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	5 mils	25 mils	24.9 Ω ±1%	Max = 600 mils

(#543016) DDI Disabling and Termination Guidelines

Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC

3D3V_S0
SIO_EXT_SMI# 1 R402 2 10KR2J-3-GP

Add RTC Gen 9 reset circuit_20170814 leakage issue

3D3V_S5_PCH
R406 10KR2J-3-GP
RTC_RST
3D3V_S5_PCH
R405 10KR2J-3-GP
RTC_RST
RO13_20171011
Q401 2N7002KDW-1-GP
common part
75.27002.F7C
2nd = 075.27002.0E7C
DP1_HPD_CPU_R
DP1_HPD_CPU
CPU_DP_HPD_P
RTC_RST
DY
R407 100KR2J-1-GP
SB 0403

Layout Placement Request
RTC Gen 9 reset circuit_20170814
DP1_HPD_CPU_R
R403 100KR2J-1-GP
DP for Type-C Mux

Jedi UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

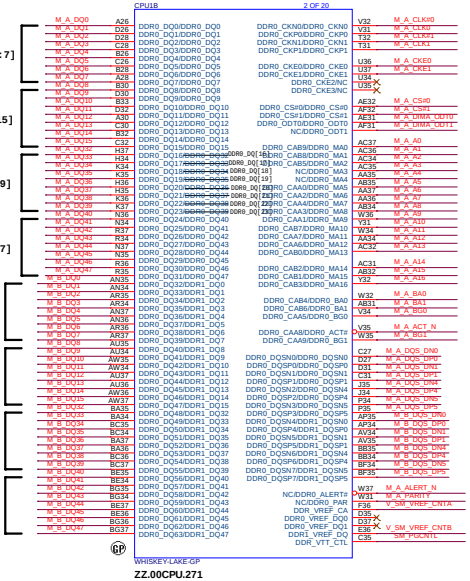
Title: CPU (DDI/EDP)

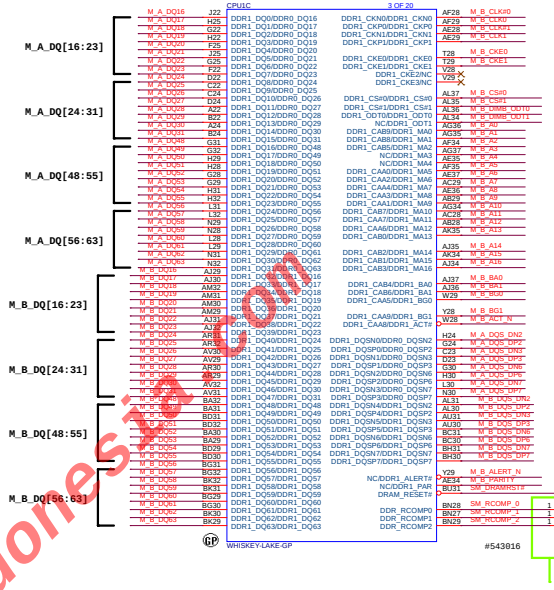
Size	Document Number	Rev
A2	Jedi15"/17" WHL-U	A00

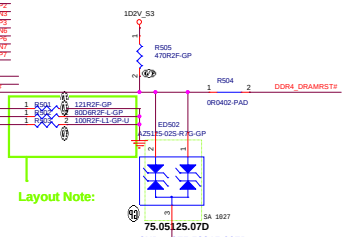
Date: Tuesday, January 08, 2019 Sheet 4 of 106

Main Func = CPU

DDR4 ball type: NON-Interleaved Type

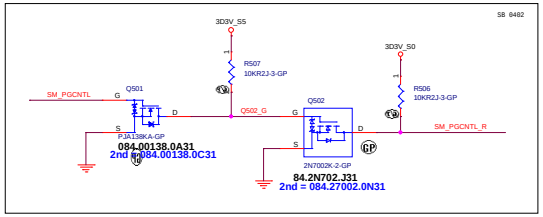






Design Guideline:
SM_RCOMP keep routing length less than 500 mils.

Layout Note:



DQ Bit Swapping is allowed within the same byte, and Byte Swapping is allowed within the same channel.
Clock (CLK and CLK#) and Strobe (DQS and DQS#) differential signal swapping within a pair is not allowed. Also differential clock pair to clock pair swapping within a channel is not allowed.

PDG: DDR/ODT

4.3 ODT Connectivity

Table 4-19. ODT Signals Connectivity Table

Processor	Memory type	Side	Signal	Rule
WHL-U	DDR4 Memory Down	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[0] connected to DRAMs' Rank0 ODT. Processor's ODT[1] connected to DRAMs' Rank1 ODT balls. If Rank1 not used, Processor ODT[1] not connected.
		DRAMs	ODT[1:0]	
	DDR4 SODIMM	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[1:0] balls connected to DIMM ODT[1:0] balls.
		DIMMs	ODT[1:0]	

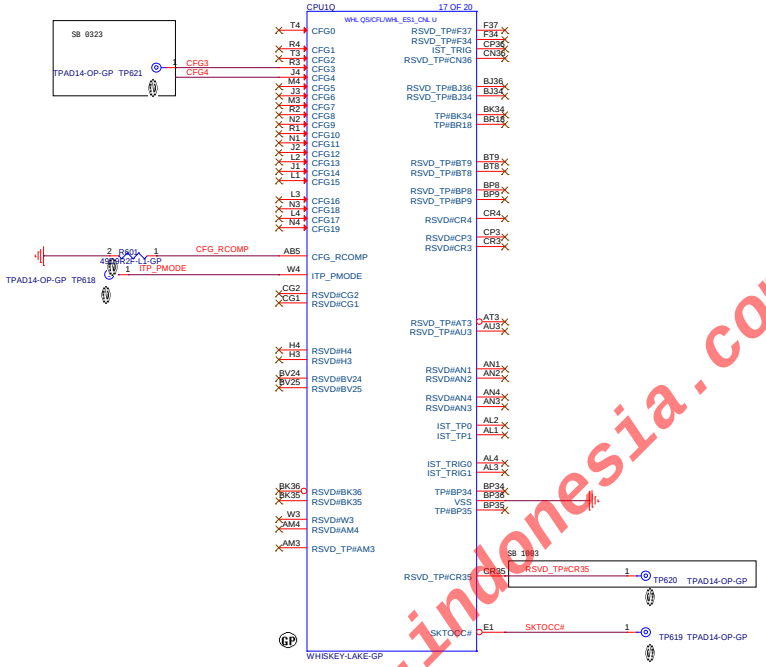
Note:
1. For additional ODT signal connection details reference the Customer Reference Board (CRB) schematics and board files.

Jedi UMA/DIS 2IN1

Wistron Corporation
2/F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (DDR)
Size: Custom | Document Number: Jedi15"/17" WHL-U | Rev: A00
Date: Tuesday, January 08, 2019 | Sheet 5 of 105

Main Func = CPU



SKL(#543016):
Processor strap CFG[4] should be pulled low to enable embedded DisplayPort*

Jedi UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (CFG/IST)

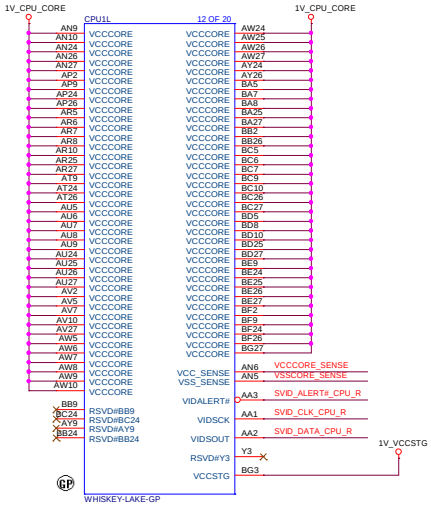
Size: A2 | Document Number: Jedi15"/17" WHL-U | Rev: A00

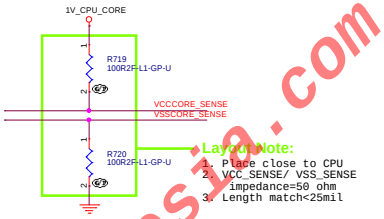
Date: Tuesday, January 08, 2019 | Sheet 6 of 106

Main Func = CPU

46 VCCCORE_SENSE
46 VSSCORE_SENSE

46 VIDSOUT_CPU_R
46 VIDSCK_CPU_R
46 PWR_VCORE_ALERT#



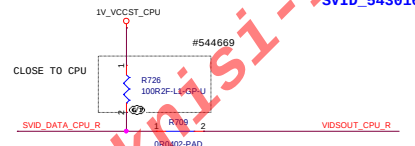


Layout Note:
1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Length match<25mil

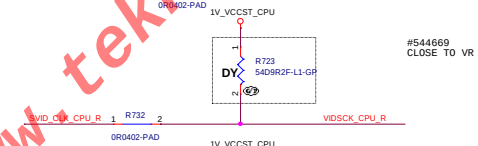
Layout Note:
The total Length of Data and Clock (from CPU to each VR) must be equal (±0.1 inch).
Route the Alert signal between the Clock and the Data signals.

SVID_543016:

SVID DATA



SVID CLOCK



SVID ALERT

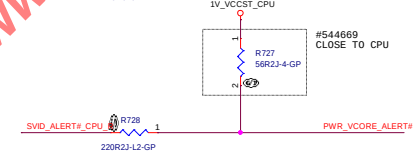


Figure 7-19. Routing Illustration for SVID Topology

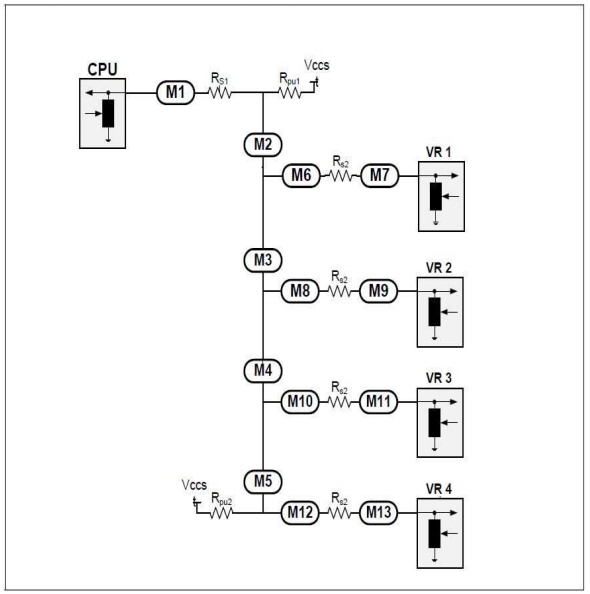


Table 7-18. SVID# Routing Guidelines (Sheet 2 of 2)

Segment	Tline Type	Reference	Via Count	Max Length, mm		Max Length, Mils	
				Segment	Total	Segment	Total
M2	MS/SL/DSL	VSS		381	432	15000	17007.9
M3	MS/SL/DSL	VSS		102		4015.75	
M4	MS/SL/DSL	VSS		102		4015.75	
M5	MS/SL/DSL	VSS		102		4015.75	
M6	MS/SL/DSL	VSS		3	3	118.11	118.11
M7	MS/SL/DSL	VSS		3	3	118.11	118.11
M8	MS/SL/DSL	VSS		3	3	118.11	118.11
M9	MS/SL/DSL	VSS		3	3	118.11	118.11
M10	MS/SL/DSL	VSS		3	3	118.11	118.11
M11	MS/SL/DSL	VSS		3	3	118.11	118.11
M12	MS/SL/DSL	VSS		3	3	118.11	118.11
M13	MS/SL/DSL	VSS		3	3	118.11	118.11
Topology Guidelines							
SVID Signals	VIDSOUT, VIDSCK, VIDSALERT#						
VIDSOUT platform resistors	Rpu1=100Ω, Rpu2=100Ω, Rs1=0Ω, Rs2=10Ω						
VIDSCK platform resistors	Rpu1=Empty, Rpu2=45Ω, Rs1=0Ω, Rs2=49.9Ω						
VIDSALERT# platform resistors	Rpu1=56Ω, Rpu2=Empty, Rs1=220Ω, Rs2=0Ω						
Platform resistors tolerances	± 5%						
Route ordering	When routing at minimum spacing route Alert between Data and Clock						
Length Matching Rules							
Length Matching between VIDSOUT and VIDSCK	± 100mils						

Jedi UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

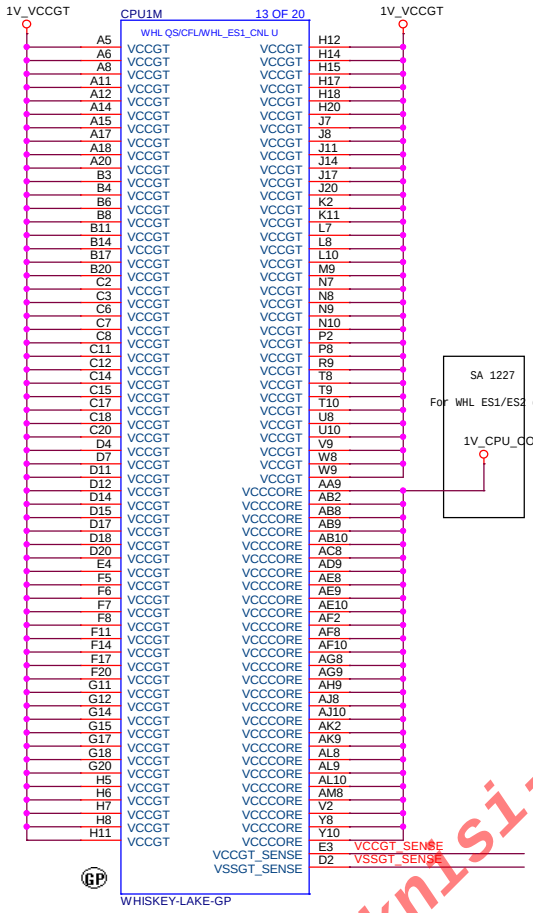
Title: CPU (VCORE/VID)
Size: A2
Document Number: Jedi15"/17" WHL-U
Rev: A00
Date: Tuesday, January 08, 2019
Sheet 7 of 106

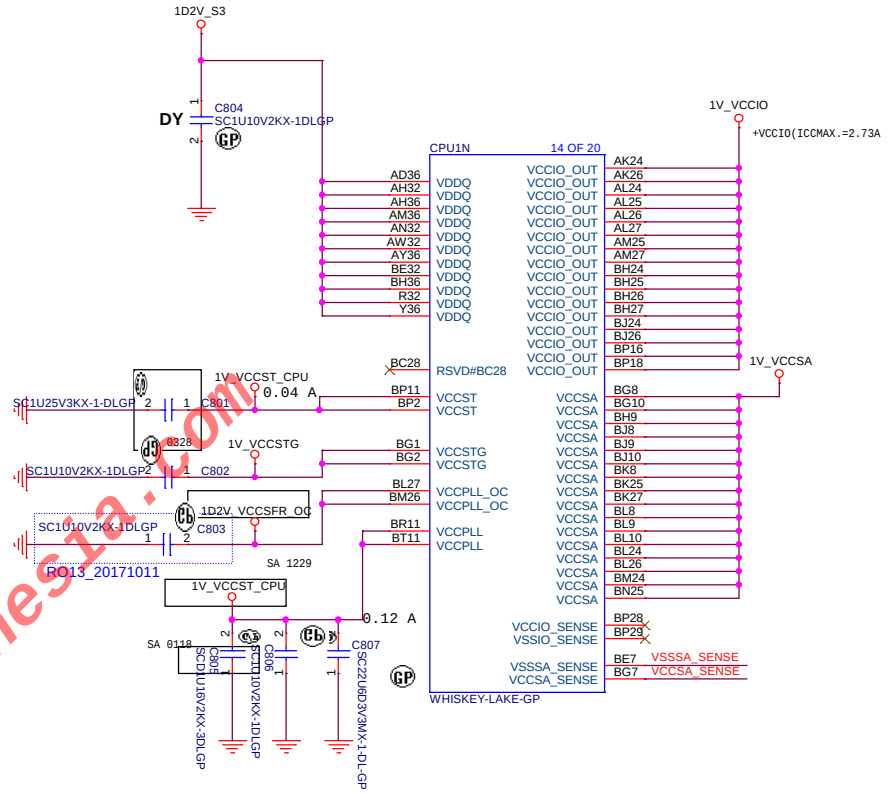
Main Func = CPU

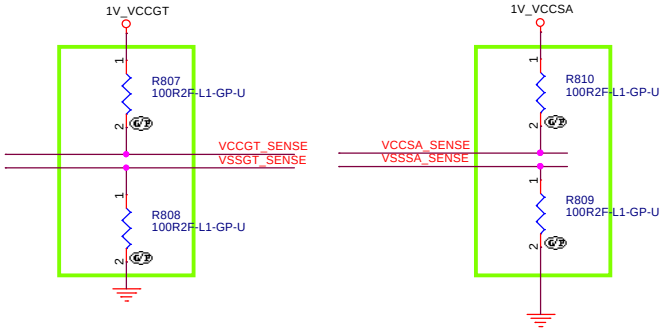
46 VSSSA_SENSE
46 VCCSA_SENSE
46 VCCGT_SENSE
46 VSSGT_SENSE

Pin Number	CFL-U43E	WHL ES1 Netname	WHL ES2 Netname
AA9	VCCGT	VCCGT	VCCCORE
AB10	VCCGT	VCCGT	VCCCORE
AB2	VCCGT	VCCGT	VCCCORE
AB8	VCCGT	VCCGT	VCCCORE
AB9	VCCGT	VCCGT	VCCCORE
AC8	VCCGT	VCCGT	VCCCORE
AD9	VCCGT	VCCGT	VCCCORE
AE10	VCCGT	VCCGT	VCCCORE
AE8	VCCGT	VCCGT	VCCCORE
AE9	VCCGT	VCCGT	VCCCORE
AF10	VCCGT	VCCGT	VCCCORE
AF2	VCCGT	VCCGT	VCCCORE
AF8	VCCGT	VCCGT	VCCCORE
AG8	VCCGT	VCCGT	VCCCORE
AG9	VCCGT	VCCGT	VCCCORE
AH9	VCCGT	VCCGT	VCCCORE
AJ10	VCCGT	VCCGT	VCCCORE
AJ8	VCCGT	VCCGT	VCCCORE
AK2	VCCGT	VCCGT	VCCCORE
AK9	VCCGT	VCCGT	VCCCORE
AL10	VCCGT	VCCGT	VCCCORE
AL8	VCCGT	VCCGT	VCCCORE
AL9	VCCGT	VCCGT	VCCCORE
AM8	VCCGT	VCCGT	VCCCORE
V2	VCCGT	VCCGT	VCCCORE
Y10	VCCGT	VCCGT	VCCCORE
Y8	VCCGT	VCCGT	VCCCORE

Layout Placement Request







Jedi UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VCCGT/VCCIO/VDDQ/VCCSA)

Size: A3 | Document Number: Jedi15"/17" WHL-U | Rev: A00

Date: Tuesday, January 08, 2019 | Sheet 8 of 106

(Blanking)

Jedi UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (RSVD)

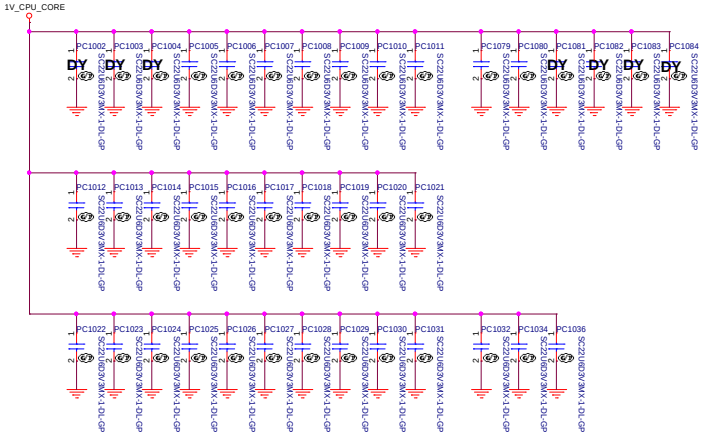
Size: A3 | Document Number: Jedi15"/17" WHL-U | Rev: A00

Date: Tuesday, January 08, 2019 | Sheet 9 of 106

Main Func = CPU

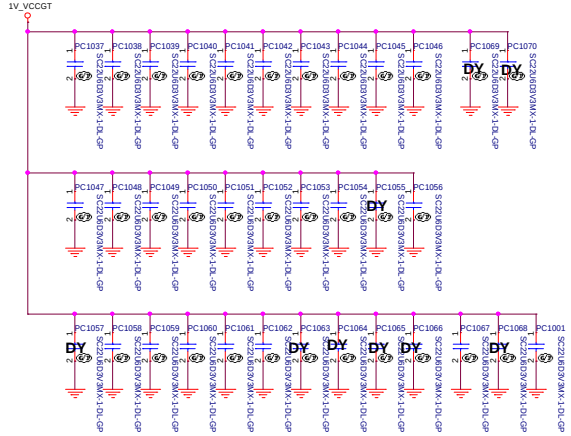
1V_CPU_CORE

22U 0603 x 39 (7DY)



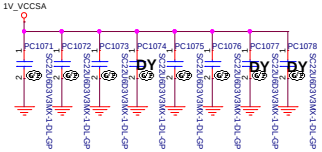
VCCGT

22U 0603 x 35 (13 DY)



VCCSA

22U 0603 x 8 (3DY)



11.3.1 Whiskey Lake U 4+2 Decoupling Requirement

Table 11-1. Whiskey Lake U 4+2 Bulk Decoupling Example

Bulk Decoupling Locations	Example	Notes
Vcc_{CORE} Power Plane at VR output	4x 220uF (@4.5mO ESR)	Placed at primary side near to VR output
Vcc_{GT} Power Plane at VR output	2x 220uF (@4.5mO ESR)	Placed at primary side near to VR output

Notes:
1. These examples are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.
2. Bulk decoupling is not a "requirement" but recommendation only. It is an example of VR design/VR bandwidth. Customer should work with respective vendor to validate their VR & bulk decoupling designs to ensure the electrical requirements are met.

Table 11-2. Decoupling Requirements for Whiskey Lake U 4+2 Processor (Sheet 1 of 2)

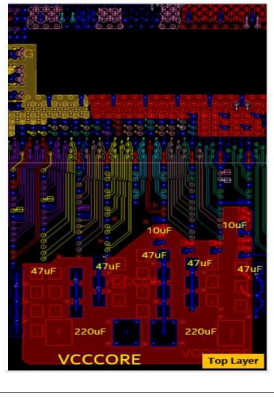
Domain	Primary Side cap	Secondary Side cap	Placement guideline
Vcc_{CORE}		42x 1uF 0402/0201	To be placed as close as possible to the vias that connect to the BGA pins.
		14x 10uF 0402	
		9x 22uF 0603	
	8x 10uF 0402		Place as close to the package as possible
	18x 47uF 0805 (6.3V)		Place as close to the package as possible. Can be placed on as either Primary or back side cap.
Vcc_{GT}	15x 22uF 0603		Place as close to the package as possible
	4x 47uF 0805 (6.3V)		
		11x 1uF 0402/0201	Place as close to the package as possible
		15x 10uF 0402	

Table 11-2. Decoupling Requirements for Whiskey Lake U 4+2 Processor (Sheet 2 of 2)

Domain	Primary Side cap	Secondary Side cap	Placement guideline
Vcc_{SA}		*4x 0402*	*Placeholder only.*
		7x 10uF 0402	
	6x 10uF 0402		
	2x 47uF 0805 (6.3V)		
	2x 0805		*Placeholder Only*
V_{DDQ}		4x 1uF 0402/0201	Place as close to the package as possible.
		3x 10uF 0402	
	1x 22uF 0603		
	6x 10uF 0402		
Vcc_{IO}	4x 1uF 0201		Place as close to the package as possible
	6x 10uF 0402		Place as close to the package as possible
	4x 0402		*Placeholder Only*
Vcc_{PLL_OC}	1x 1uF 0402		Do not merge Vcc_{PLL}, Vcc_{PLL_OC} and Vcc_{ST} to any noisy and high current power rail and do not route them close/ adjacent to and reference to, any noisy and high current rail on top and bottom layers - as this may impact to PLL failing to phase lock.
Vcc_{PLL}	1x 0.1uF 0201		Place as close as possible to BGA.
	1x 1uF 0402		Place as close as possible to BGA and can be placed on as either Primary or backside cap.
	1x 0805		*Placeholder Only.* Can be placed on as either Primary or back side cap.
Vcc_{ST}	1x 1uF 0402		
Vcc_{STG}	1x 1uF 0402		

Notes:
1. The 6.3V voltage is for the higher capacitance retention; more 0805 components will be required for a lower voltage capacitor rating. Assumption: VR loop bandwidth ' 250kHz e.g., 1MHz switching VR
2. Component placement order: Package edge > 0402 caps > 0603 caps > 0805 caps > Bulk caps >Power source.

Figure 11-8. Whiskey Lake U 4+2 Vcc_{CORE} Routing Guideline



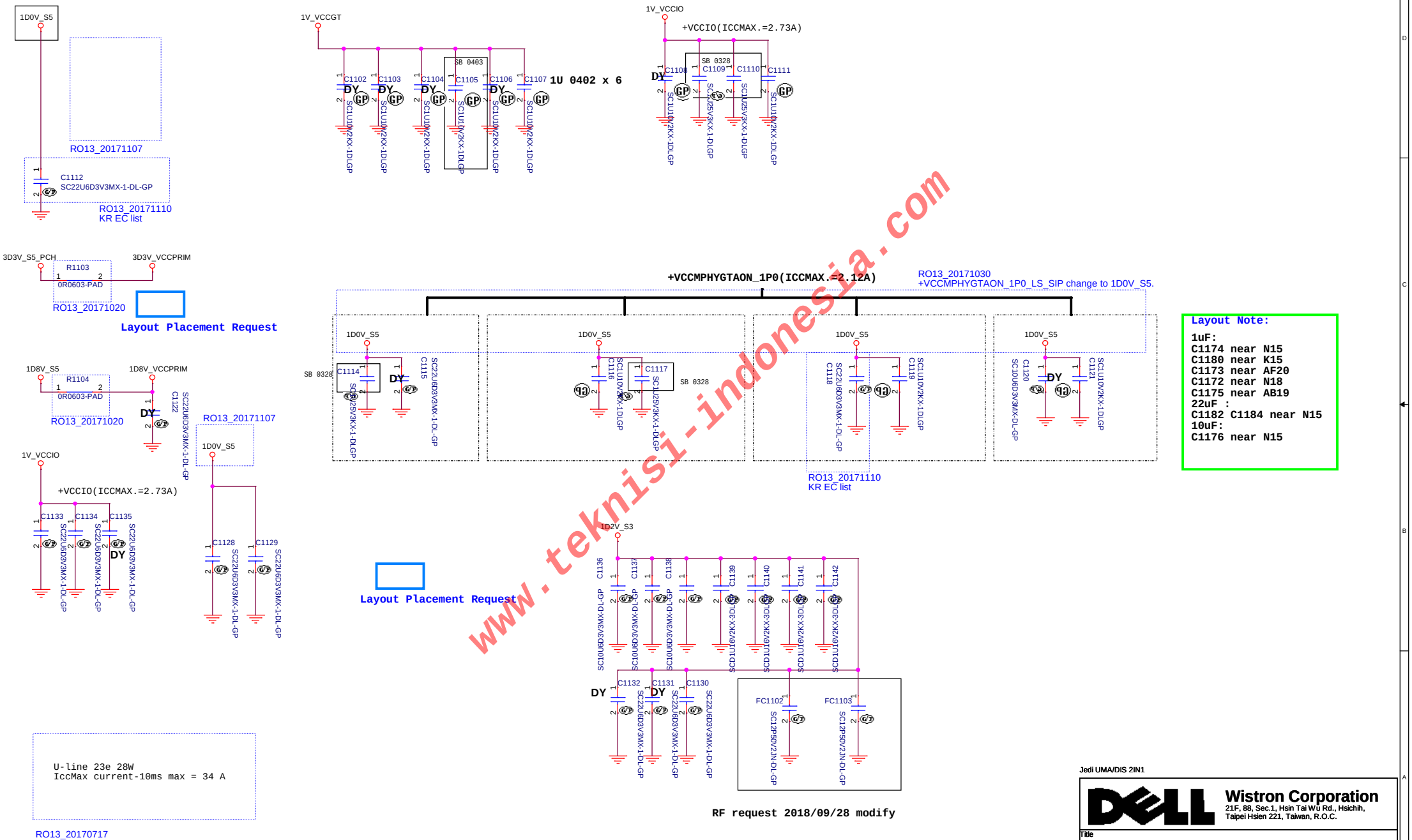
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (Power CAP1)
Size: A2 | Document Number: Jedi15"/17" WHL-U | Rev: A00
Date: Tuesday, January 08, 2019 | Sheet 10 of 106

Main Func = CPU

PCH DERIVED RAILS UNSLICED GT VCCIO



Jedi UMA/DIS 2IN1

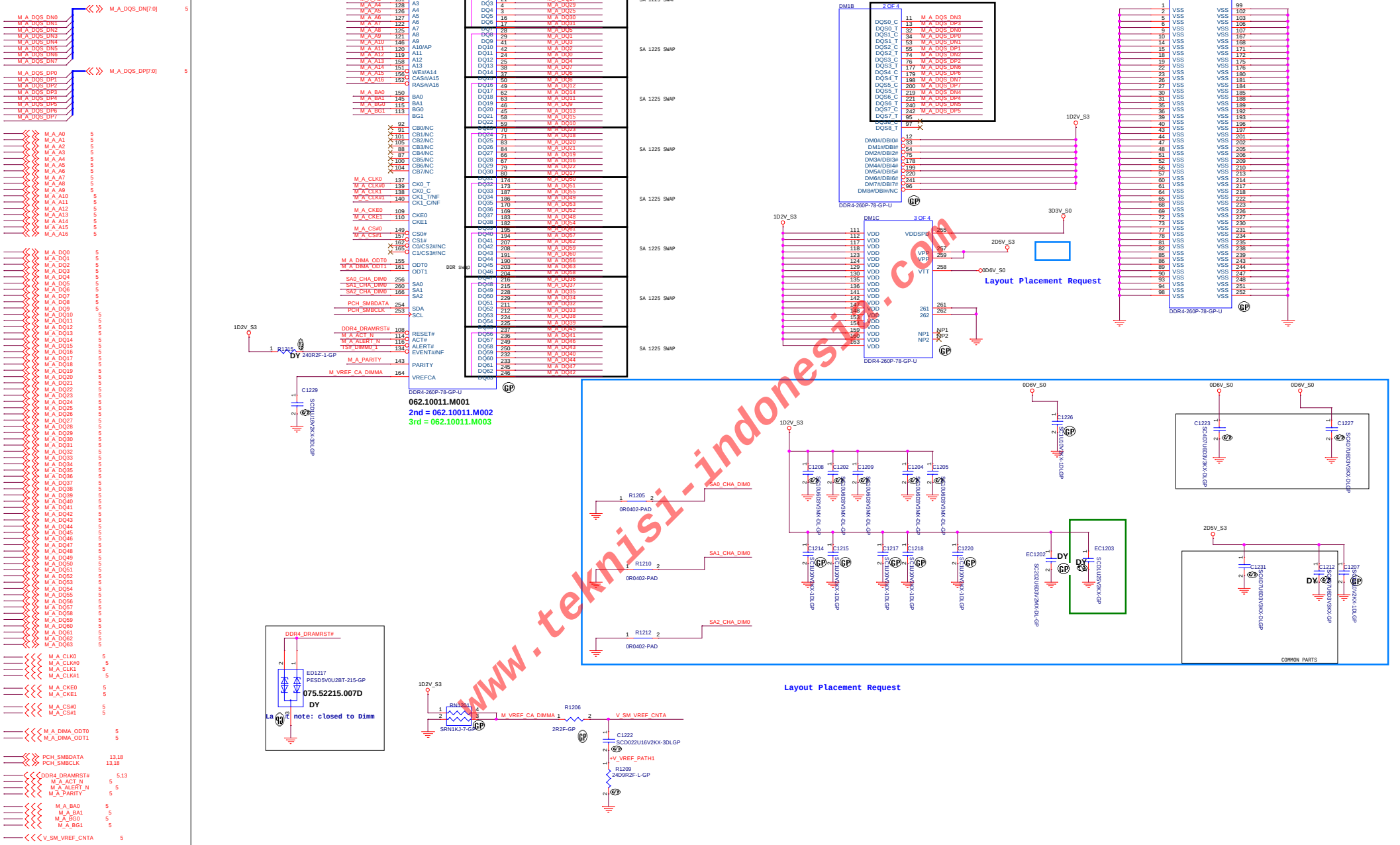
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (Power Cap2)

Size	Document Number	Rev
A3	Jedi15"/17" WHL-U	A00

Date: Tuesday, January 08, 2019 Sheet 11 of 106

Main Func = MEMORY



Jedi UMA/DIS 2IN1

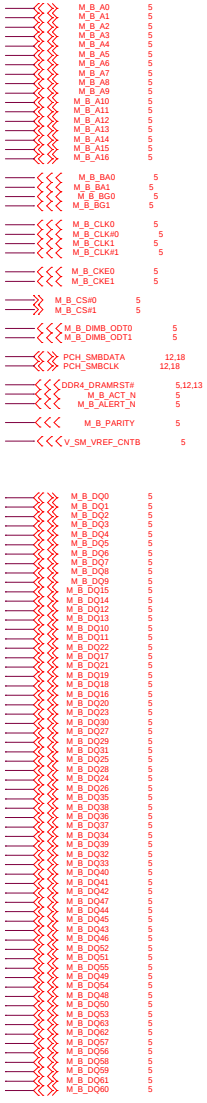
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

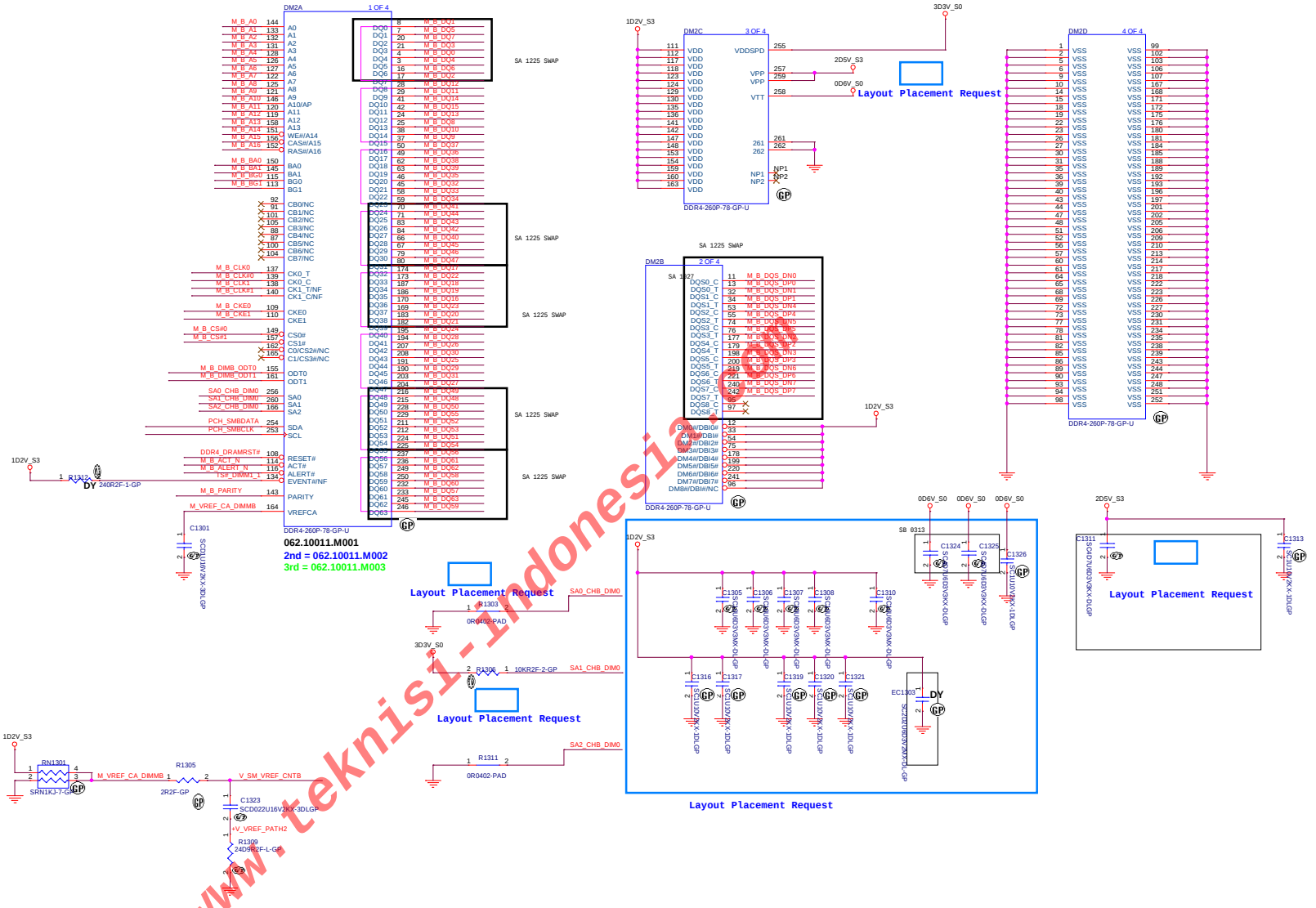
Title: DDR (DDR4-CHA)

Size: A2 | Document Number: Jedi15"/17" WHL-U | Rev: A00

Date: Tuesday, January 08, 2019 | Sheet 12 of 106

Main Func = MEMORY





Jedi UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR (DDR4-CHB)

Size	Document Number	Rev
A2	Jedi15"/17" WHL-U	A00

Date: Tuesday, January 08, 2019 Sheet 13 of 106

(Blanking)

Jedi UMA/DIS 2IN1

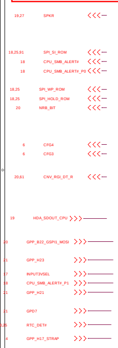
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR (RSVD) (DDR4-CHA1)

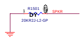
Size	Document Number	Rev
A4	Jedi15"/17" WHL-U	A00

Date: Tuesday, January 08, 2019 Sheet 14 of 106

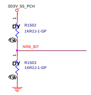
Main Func = PCH



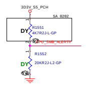
GPP_B14 / SPKR	Top Swap Override	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "Top Swap" mode. (Default) 1 = **Enable** "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64-KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap (See SPI Flash Programming Guide). ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. Software will not be able to clear the Top Swap bit until the system is rebooted. 3. The status of this strap is readable using the Top Swap bit (Bus0, Device31, Function0, offset DCh, bit4). 4. This signal is in the primary well.



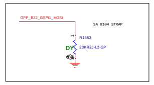
GPP_B18 / GSPIO_MOSI	No Reboot	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "No Reboot" mode. (Default) 1 = **Enable** "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.



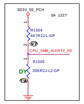
GPP_C2 / SMBALERT#	TLS Confidentiality	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **Disable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) 1 = **Enable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.



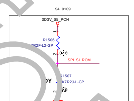
GPP_B22 / GSPI1_MOSI	Boot BIOS Strap Bit BBS	Rising edge of PCH_PWROK	This Signal has a weak internal pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device31, Function0, offset DCh, bit 6). **Bit 6** / **Boot BIOS Destination** 0 — SPI (Default) 1 — LPC ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. 3. Boot BIOS Destination select to LPC by functional strap or using Boot BIOS Destination bit will not affect SPI accesses initiated by Intel ME or Integrated GbE LAN. 4. This signal is in the primary well.



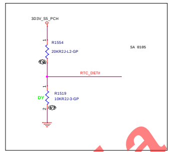
GPP_C5 / SML0ALERT#	eSPI or LPC	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **LPC** is selected (for EC). (Default) 1 = **eSPI** is selected (for EC). ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. ***Warning:*** **If this strap is configured to '0' (eSPI is disabled), the e*SPI Flash Sharing Mode* strap must be configured to '0' as well (SAFS is disabled)**



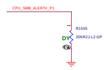
SPI0_MOSI	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.



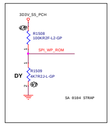
GPP_D12 / ISH_SPI_MOSI / GSPI2_MOSI	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.



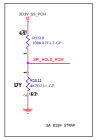
GPP_B23 / SML1ALERT# / PCHHOT#	Intel® DCI-OOB	Rising edge of RSMRST#	This signal has an internal pull-down. 0 = Disable Intel® DCI-OOB (Default) 1 = Enable Intel® DCI-OOB ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. When used as PCHHOT# and strap low, a 150K pull-up is needed to ensure it does not override the internal pull-down strap sampling. This signal is in the primary well.



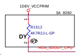
SPI0_IO2	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.



SPI0_IO3	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.



HDA_SDO / I2S0_TXD	Flash Descriptor Security Override	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = **Enable** security measures defined in the Flash Descriptor. (Default) 1 = **Disable** Flash Descriptor Security (override). This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.



GPP_E19 / DDPB_CTRLDATA / CNV_BT_IF_SELECT	Display Port B Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down . 0 = Port B is not detected. (Default) 1 = Port B is detected. ***Notes:*** 1. The internal Pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

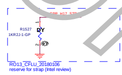
Page 4 RN401 2.2K PU 3.3V_S0

GPP_E21 / DDPC_CTRLDATA	Display Port C Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down. 0 = Port C is not detected. (Default) 1 = Port C is detected. ***Notes:*** 1. The internal Pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

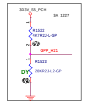
GPP_E23 / DDPD_CTRLDATA	Display Port D Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port D is not detected. (Default) 1 = Port D is detected. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

Page 4 RN403 2.2K PU 3.3V_S0

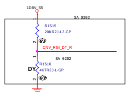
GPP_H17	Reserved	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.



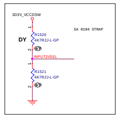
GPP_H21	XTAL Frequency Select	Rising edge of RSMRST#	This signal has a weak internal pull-down. An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH. 0 = 38.4 XTAL frequency selected. (Default) 1 = 24MHz XTAL frequency selected. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.



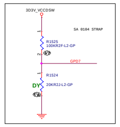
GPP_F6 / CNV_RGI_DT	M.2 CNV Mode Select	Rising edge of RSMRST#	An external pull-up or pull-down is required. 0 = Integrated CNVi enable. 1 = Integrated CNVi disable.



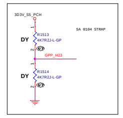
INPUT3VSEL	3.0V Select	Input pin must always be driven to a valid logic level	External pull-up or pull-down is required 0 = 3.3V supply is 3.3V +/- 5% 1 = 3.3V supply is 3.0V +/- 5% **Note:** This strap should only be used for specific targeted 1S battery systems.



GPD7	Reserved	Rising edge of DSW_PWROK	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling

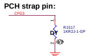


GPP_H23	eSPI Flash Sharing Mode	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = Master Attached Flash Sharing (MAFS) enabled (Default) 1 = Slave Attached Flash Sharing (SAFS) enabled. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. ***Warning:*** **This strap must be configured to '0' (SAFS is disabled) if the *eSPI or LPC* strap is configured to '0' (eSPI is disabled)**



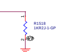
[BDW Only]PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR
	1 : DISABLED

PCH strap pin:



(#543016)

DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED An external Display Port device is connected to the Embedded Display Port. 1 : DISABLED (Default) No Physical Display Port attached to Embedded DisplayPort*. No connect for disable.



DELL Wistron Corporation
CPU (STRAP)
Jedi15"/17" WHL-U
A00

Main Func = PCH

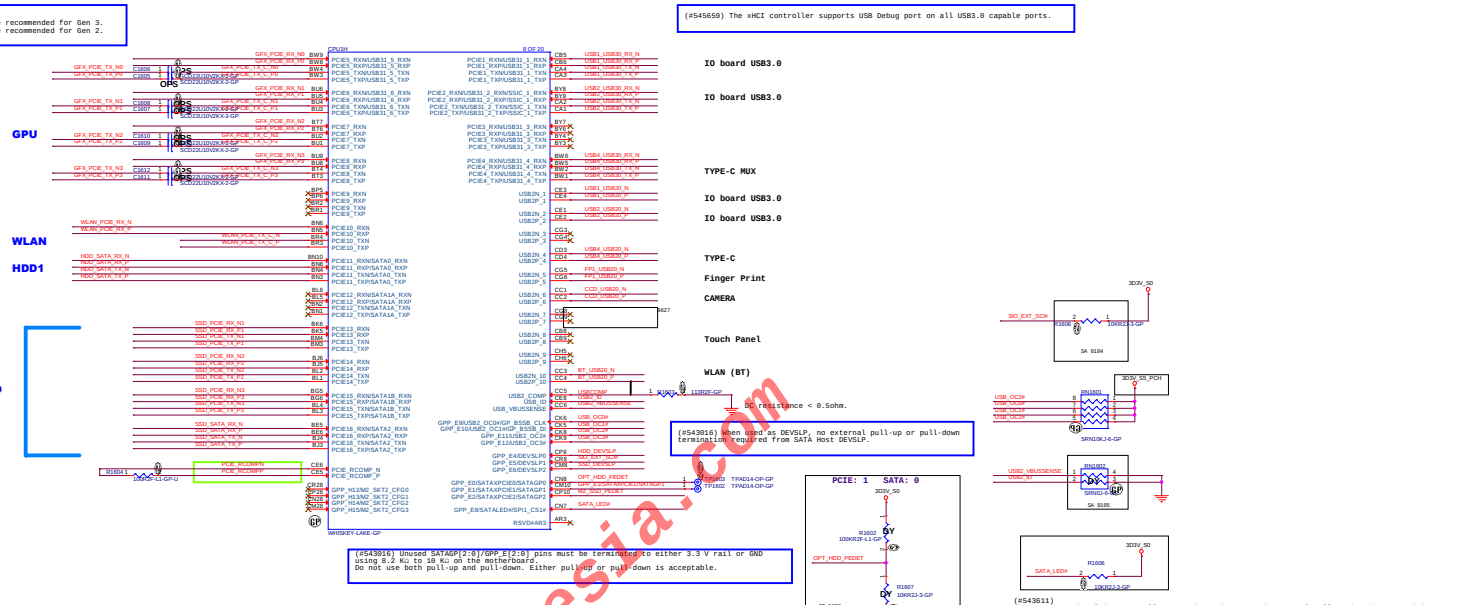


Figure 6-1. High Speed I/O (HSIO) Lane Multiplexing in CNL U PCH-LP

6.3.1 PCH PCI Express* Interface Configuration Details

Figure 6-2. Supported PCH PCI Express* Link Configurations

PCH-LP		PCIe* Controller #1				PCIe* Controller #2				PCIe* Controller #3				PCIe* Controller #4			
										Cycle Router #2				Cycle Router #3			
Flex I/O Lane		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
PCIe* Lane		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Premium-U	1x4	RP1				RP5				RP9				RP13			
	1x4 LR	RP1				RP5				RP9				RP13			
	2x2	RP1		RP3		RP5		RP7		RP9		RP11		RP13		RP15	
	1x2+2x1	RP1		RP3	RP4	RP5		RP7	RP8	RP9		RP11	RP12	RP13		RP15	RP16
	2x1+1x2	RP4	RP3	RP1		RP8	RP7	RP5		RP12	RP11	RP9		RP16	RP15	RP13	
	4x1	RP1	RP2	RP3	RP4	RP5	RP6	RP7	RP8	RP9	RP10	RP11	RP12	RP13	RP14	RP15	RP16

Jedi USM/DIS 29N1

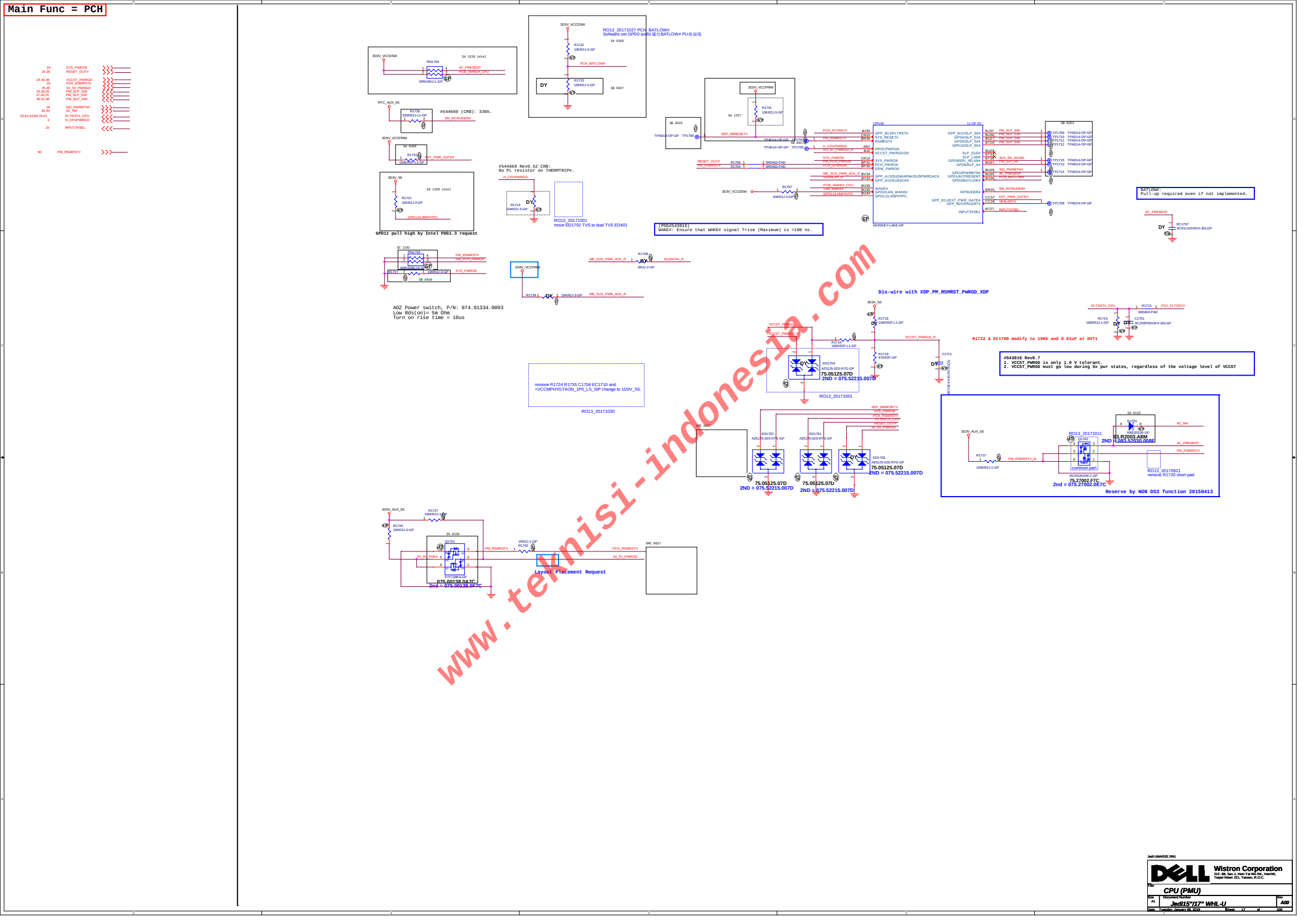
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PCIE/SATA/USB)

Size	Document Number	Rev
A1	Jedi15"/17" WHL-U	A00

Date: Tuesday, January 08, 2019 Sheet 16 of 106

Main Func = PCH



Jedi UMA/DIS 29N1

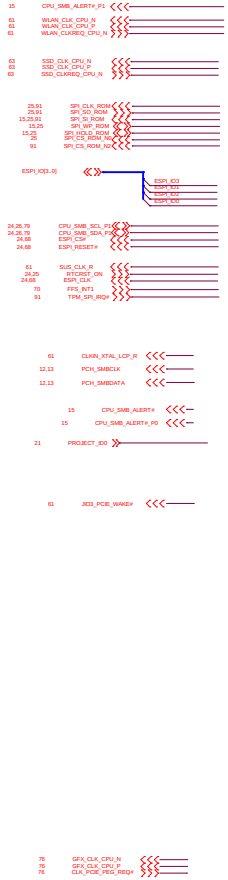
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

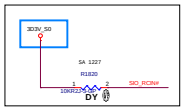
CPU (PMU)

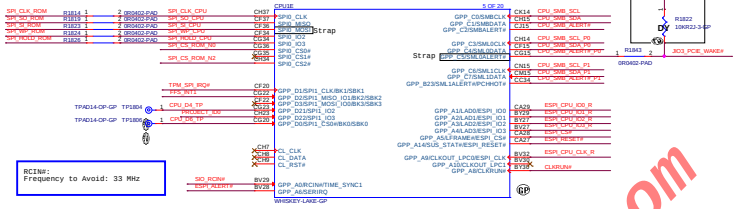
Size	Document Number	Rev
A1	Jedi15"/17" WHL-U	A00

Date: Tuesday, January 09, 2018 Sheet 17 of 106

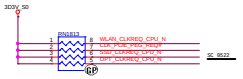
Main Func = PCH

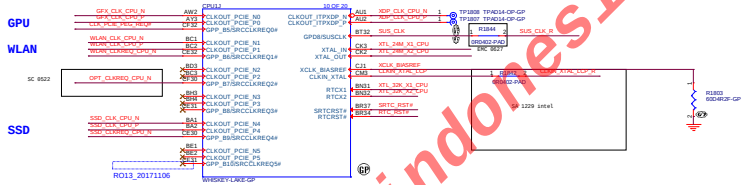


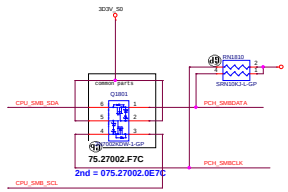


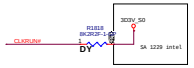


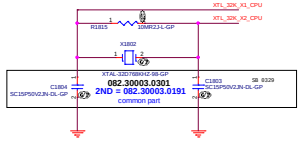
RCIN#:
Frequency to Avoid: 33 MHz

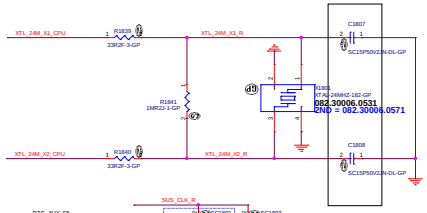


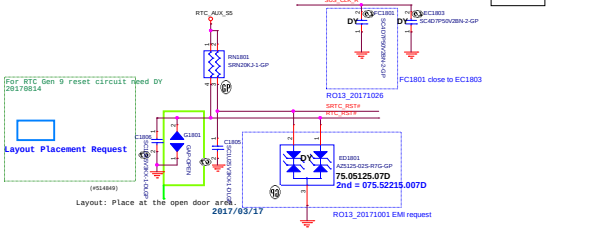












For eSPI

CPU_SMB_ALERT#_P0

Table 3: Platform Supported Pin Strap Settings for LPC / eSPI / SPI Flash

ESPI Enable Strap (ESPI_EN) Value (0: LPC, 1: eSPI)	Boot BIOS Strap (BBS) Value (0: SPI, 1: LPC/eSPI)	EC Connection	Boot (BIOS) Flash Connection (section 3.1.4)
0	0	LPC	SPI
0	1	LPC	LPC
1	0	eSPI	SPI
1	1	eSPI	eSPI (to EC over eSPI Peripheral Channel) (refer to Section 3.1.4 for details)

PCH strap pin:

eSPI or LPC	Sampled at rising edge of RSMRST#
SML0ALERT# / GPP_C5	This signal has a weak internal pull-down. 0 = LPC is selected for EC. 1 = eSPI is selected for EC.

This signal has a weak internal pull-down.

Table 9-1. Functional Strap Definitions (Sheet 2 of 3)

Signal	Usage	When Sampled	Comment
GSPI1_MOSI/ GPP_B22	Boot BIOS Strap Bit BBS	Rising edge of PCH_PWROK	This Signal has a weak internal Pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device31, Function0, offset BCh, bit 6). **Bit 6 — Boot BIOS Destination** 0 — SPI (Default) 1 — LPC ***Notes:*** 1. The internal Pull-down is disabled after PLTRST# de-asserts. 2. If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. 3. Boot BIOS Destination select to LPC by functional strap or using Boot BIOS Destination bit will not affect SPI accesses initiated by Intel ME or Integrated GbE LAN. 4. This signal is in the primary well.
SML0ALERT# / GPP_C5	eSPI or LPC	Rising edge of RSMRST#	This signal has a weak internal Pull-down. 0 = **LPC** is selected for EC. (Default) 1 = **eSPI** is selected for EC. ***Notes:*** 1. The internal Pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

Jedi UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

File: CPU (SPI/ESPI/SMBS/XTAL/CLK)

Size	Document Number	Rev
A1	Jedi15"/17" WHL-U	A00

Date: Tuesday, January 09, 2018 Sheet 18 of 106

Main Func = PCH

61 BT_PCMFRM_RSTN
61 BT_PCMOUT_CLKREQ0
55 DMIC_PCH_DATA
55 DMIC_PCH_CLK
15,27 SPKR
27 HDA_SDIN0_CPU
27 HDA_SYNC_CODEC
27 HDA_BITCLK_CODEC
68 ME_FWP_SW
27 HDA_SDOUT_CODEC
65 KB_LED_BL_DET
15 HDA_SDOUT_CPU
24,85 DGPU_PWROK

33 SD_SDATA0
33 SD_SDATA1
33 SD_SDATA2
33 SD_SDATA3
33 SD_CMD
33 SD_WP
33 SD_CD_N
33 SD_CLK
33 SD_PWR_EN#

DGPU_PWROK
R1924 100KR2J-1-GP
SC 1121

3D3V_S5
fTPM
R1910 10KR2J-3-GP
TPM_ID
TPM
R1911 10KR2J-3-GP

CPU1G 7 OF 20
HDA_SYNC_CPU BN34 HDA_SYNC/I2S0_SFRM
HDA_BITCLK_CPU BN37 HDA_BCLK/I2S0_SCLK
HDA_SDOUT_CPU BN36 HDA_SDO/I2S0_TXD
HDA_SDIN0_CPU BN35 HDA_SDI0/I2S0_RXD
HDA_RST_N_CPU BL36 HDA_SDI1/I2S1_RXD/SNDW1_DATA
BL35 HDA_RST#/I2S1_SCLK/SNDW1_CLK
KB_LED_BL_DET CK23 GPP_D23/I2S_MCLK
BL37
BL34 I2S1_SFRM/SNDW2_CLK
I2S1_TXD/SNDW2_DATA
GPP_G0/SD_CMD CH36 SD_CMD
GPP_G1/SD_DATA0 CL35 SD_SDATA0
GPP_G2/SD_DATA1 CL36 SD_SDATA1
GPP_G3/SD_DATA2 CM35 SD_SDATA2
GPP_G4/SD_DATA3 CN35 SD_SDATA3
GPP_G5/SD_CD# CH35 SD_CD_N
GPP_G6/SD_CLK CK36 SD_CLK
GPP_G7/SD_WP CK34 SD_WP
TPAD14-OP-GP TP1903
BT_PCMFRM_RSTN R1923 33R2J-2-GP GPP_H1_SFRM CJ32 GPP_H1/I2S2_SFRM/CNV_BT_I2S_BCLK/CNV_RF_RESET#
BT_PCMOUT_CLKREQ0 R1922 33R2J-2-GP GPP_H2_CLKREQ0 CH32 GPP_H0/I2S2_SCLK/CNV_BT_I2S_SCLK
CH29 GPP_H2/I2S2_TXD/CNV_BT_I2S_SDI/MODEM_CLKREQ
CH30 GPP_H3/I2S2_RXD/CNV_BT_I2S_SDO
SA 1229 intel
SA 1229
DMIC_PCH_CLK CP24 GPP_A17/SD_VDD1_PWR_EN#/ISH_GP7
DMIC_PCH_DATA CN24 GPP_D19/DMIC_CLK0/SNDW4_CLK GPP_A16/SD_1P8_SEL
GPP_D20/DMIC_DATA0/SNDW4_DATA
TPM_ID CK25 SD_1P8_RCOMP
DGPU_PWROK CJ25 GPP_D17/DMIC_CLK1/SNDW3_CLK SD_3P3_RCOMP
GPP_D18/DMIC_DATA1/SNDW3_DATA
SPKR CF35 GPP_B14/SPKR
WHISKEY-LAKE-GP
BW36 SD_PWR_EN#
BY31
CK33 SD_RCOMP
CM34
R1901 1 2.200R2F-L-GP
RO13_CFLU_20171207

EMC 0627
EC1901 DY HDA_BITCLK_CODEC
SC10P50V2JN-4DLGP

PCH strap pin:

Flash Descriptor Security Overide/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default High = Enable *

The internal pull-down is disabled after PLTRST# deasserts

PCH strap pin: SPKR

TOP SWAP OVERRIDE	
HDA_SPKR	* High = TOP SWAP ENABLED Low = DISABLED (WEAK INTERNAL PD)

The internal pull-up
RO13_CFLU_20171212

RO13_20171027
delete ED1901

HDA_SYNC_CODEC R1908 1 2 0R0402-PAD HDA_SYNC_CPU

R1920~R1921 need to close for merge prepare

HDA_BITCLK_CODEC R1920 1 0R0402-PAD HDA_BITCLK_CPU
HDA_SDOUT_CODEC R1921 1 33R2J-2-GP HDA_SDOUT_CPU
SA 1229 intel
ME_FWP_SW R1909 1 1KR2J-1-GP

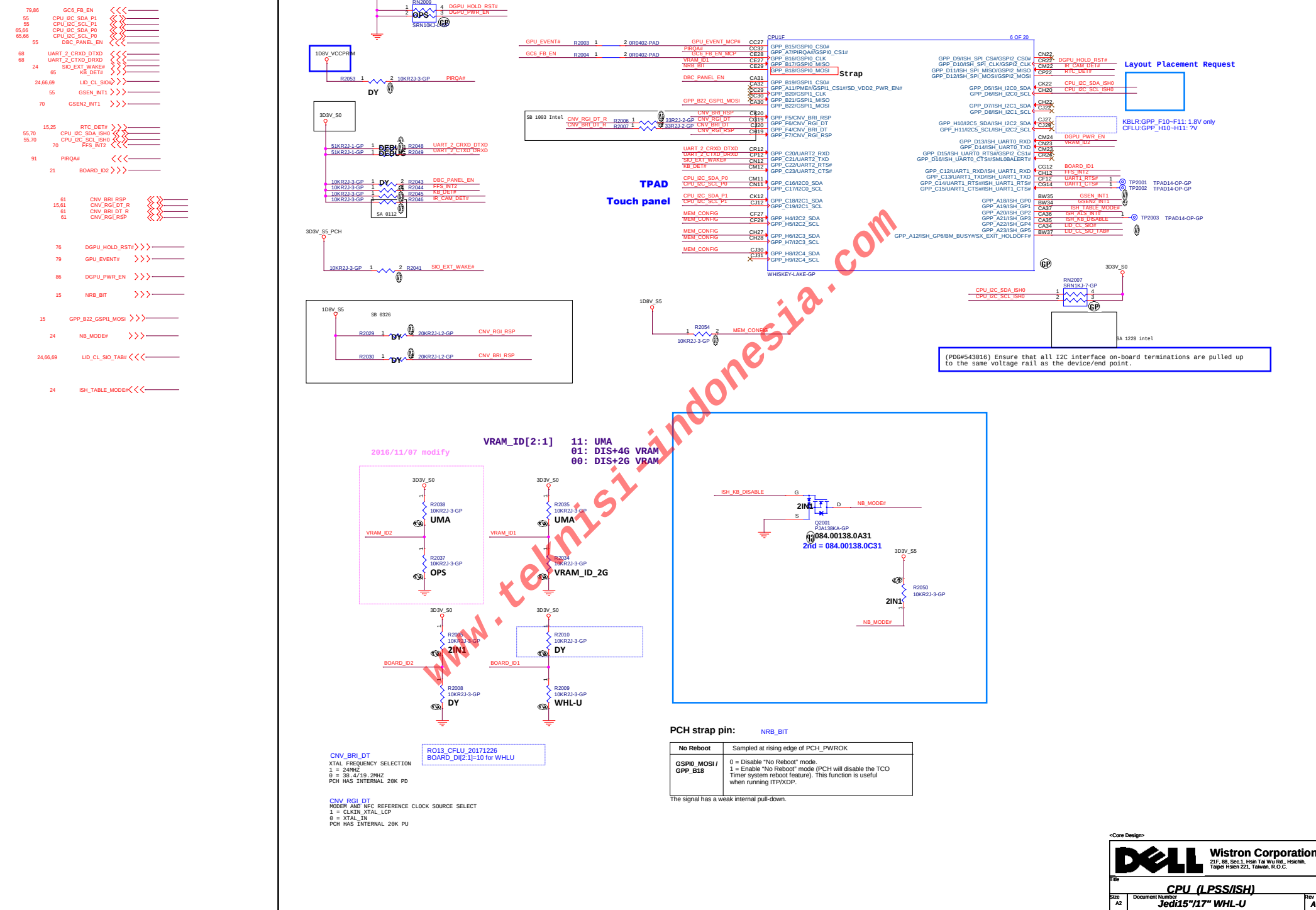
HDA_SDOUT_CODEC
EC1903 DY
SC27P50V2JN-3DLGP

Jedi UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (HAD/I2S/SD/DMIC)
Size: A2 | Document Number: Jedi15"/17" WHL-U | Rev: A00
Date: Tuesday, January 08, 2019 | Sheet 19 of 106

Main Func = PCH



EC2002 DY 1 DGPU_HOLD_RST# C1KP50V2KX-1DLGP
RN2009 OPS DGPU_HOLD_RST# DGPU_PWR_EN SRN10KJ-7-GP

1D8V_VCCPRM R2053 DY 10KR2J-3-GP PIRQA#

3D3V_S0 51KR2J-1-GP DEBUG R2048 UART_2_CRXD_DTXD
51KR2J-1-GP DEBUG R2049 UART_2_CTXD_DRXD
10KR2J-3-GP DY R2043 DBC_PANEL_EN
10KR2J-3-GP R2044 FFS_INT2
10KR2J-3-GP R2045 KB_DET#
10KR2J-3-GP R2046 IR_CAM_DET#
SA 0112

3D3V_S5_PCH 10KR2J-3-GP R2041 SIO_EXT_WAKE#

1D8V_S5 SB 0326
R2029 DY 20KR2J-L2-GP CNV_RGI_RSP
R2030 DY 20KR2J-L2-GP CNV_BRI_RSP

GPU_EVENT# R2003 0R0402-PAD GPU_EVENT_MCP#
GC6_FB_EN R2004 0R0402-PAD PIRQA#
GC6_FB_EN_MCP
VRAM_ID1
NRB_BIT
DBC_PANEL_EN
GPP_B22_GSPI1_MOSI

SB 1003 Intel
CNV_RGI_DT_R R2006 33R2J-2-GP CNV_RGI_DT
CNV_BRI_DT_R R2007 33R2J-2-GP CNV_BRI_DT
CNV_BRI_RSP
CNV_RGI_RSP

UART_2_CRXD_DTXD
UART_2_CTXD_DRXD
SIO_EXT_WAKE#
KB_DET#
CPU_I2C_SDA_P0
CPU_I2C_SCL_P0
CPU_I2C_SDA_P1
CPU_I2C_SCL_P1
MEM_CONFIG

CPU1F 6 OF 20
GPP_B15/GSPI0_CS0#
GPP_A7/PIRQA#/GSPI0_CS1#
GPP_B16/GSPI0_CLK
GPP_B17/GSPI0_MISO
GPP_B18/GSPI0_MOSI Strap
GPP_B19/GSPI1_CS0#
GPP_A11/PME#/GSPI1_CS1#/SD_VDD2_PWR_EN#
GPP_B20/GSPI1_CLK
GPP_B21/GSPI1_MISO
GPP_B22/GSPI1_MOSI
GPP_F5/CNV_BRI_RSP
GPP_F6/CNV_RGI_DT
GPP_F4/CNV_BRI_DT
GPP_F7/CNV_RGI_RSP
GPP_C20/UART2_RXD
GPP_C21/UART2_TXD
GPP_C22/UART2_RTS#
GPP_C23/UART2_CTS#
GPP_C16/I2C0_SDA
GPP_C17/I2C0_SCL
GPP_C18/I2C1_SDA
GPP_C19/I2C1_SCL
GPP_H4/I2C2_SDA
GPP_H5/I2C2_SCL
GPP_H6/I2C3_SDA
GPP_H7/I2C3_SCL
GPP_H8/I2C4_SDA
GPP_H9/I2C4_SCL
WHISKEY-LAKE-GP

GPP_D9/ISH_SPI_CS#/GSPI2_CS0# DGPU_HOLD_RST#
GPP_D10/ISH_SPI_CLK/GSPI2_CLK IR_CAM_DET#
GPP_D11/ISH_SPI_MISO/GSPI2_MISO RTC_DET#
GPP_D12/ISH_SPI_MOSI/GSPI2_MOSI
GPP_D5/ISH_I2C0_SDA CPU_I2C_SDA_ISH0
GPP_D6/ISH_I2C0_SCL CPU_I2C_SCL_ISH0
GPP_D7/ISH_I2C1_SDA
GPP_D8/ISH_I2C1_SCL
GPP_H10/I2C5_SDA/ISH_I2C2_SDA
GPP_H11/I2C5_SCL/ISH_I2C2_SCL
GPP_D13/ISH_UART0_RXD
GPP_D14/ISH_UART0_TXD
GPP_D15/ISH_UART0_RTS#/GSPI2_CS1#
GPP_D16/ISH_UART0_CTS#/SML0BALERT#
GPP_C12/UART1_RXD/ISH_UART1_RXD
GPP_C13/UART1_TXD/ISH_UART1_TXD
GPP_C14/UART1_RTS#/ISH_UART1_RTS#
GPP_C15/UART1_CTS#/ISH_UART1_CTS#
GPP_A18/ISH_GP0
GPP_A19/ISH_GP1
GPP_A20/ISH_GP2
GPP_A21/ISH_GP3
GPP_A22/ISH_GP4
GPP_A23/ISH_GP5
GPP_A12/ISH_GP6/BM_BUSY#/SX_EXIT_HOLDOFF#
DGPU_PWR_EN
VRAM_ID2
BOARD_ID1
TP2001 TPAD14-OP-GP
TP2002 TPAD14-OP-GP
GSEN_INT1
ISH_TABLE_MODE#
ISH_ALS_INT#
TP2003 TPAD14-OP-GP
ISH_KB_DISABLE
LID_CL_SIO#
LID_CL_SIO_TAB#

Layout Placement Request
KBLR:GPP_F10~F11: 1.8V only
CFLU:GPP_H10~H11: ?V

TPAD
Touch panel

1D8V_S5 R2054 10KR2J-3-GP MEM_CONFIG

3D3V_S0 RN2007 SRN1KJ-7-GP CPU_I2C_SDA_ISH0 CPU_I2C_SCL_ISH0
SA 1228 intel

(PDG#543016) Ensure that all I2C interface on-board terminations are pulled up to the same voltage rail as the device/end point.

VRAM_ID[2:1] 11: UMA
01: DIS+4G VRAM
00: DIS+2G VRAM

2016/11/07 modify

3D3V_S0 R2038 10KR2J-3-GP UMA VRAM_ID2 R2037 10KR2J-3-GP OPS
3D3V_S0 R2035 10KR2J-3-GP UMA VRAM_ID1 R2034 10KR2J-3-GP VRAM_ID_2G
3D3V_S0 R2005 10KR2J-3-GP 2IN1 BOARD_ID2 R2008 10KR2J-3-GP DY
3D3V_S0 R2010 10KR2J-3-GP DY BOARD_ID1 R2009 10KR2J-3-GP WHL-U

ISH_KB_DISABLE G 2IN1 D NB_MODE# S Q2001 PJA138KA-GP
084.00138.0A31
2nd = 084.00138.0C31
3D3V_S5 R2050 10KR2J-3-GP 2IN1 NB_MODE#

CNV_BRI_DT
XTAL FREQUENCY SELECTION
1 = 24MHZ
0 = 38.4/19.2MHZ
PCH HAS INTERNAL 20K PD

CNV_RGI_DT
MODEM AND NFC REFERENCE CLOCK SOURCE SELECT
1 = CLKIN_XTAL_LCP
0 = XTAL_IN
PCH HAS INTERNAL 20K PU

RO13_CFLU_20171226
BOARD_DI[2:1]=10 for WHLU

PCH strap pin: NRB_BIT

No Reboot	Sampled at rising edge of PCH_PWROK
GSPI0_MOSI / GPP_B18	0 = Disable "No Reboot" mode. 1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

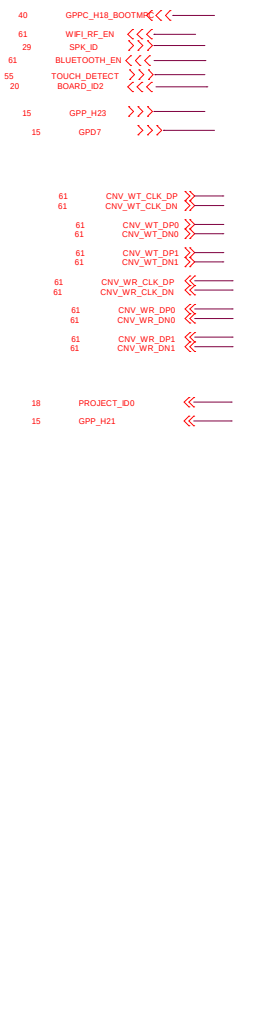
The signal has a weak internal pull-down.

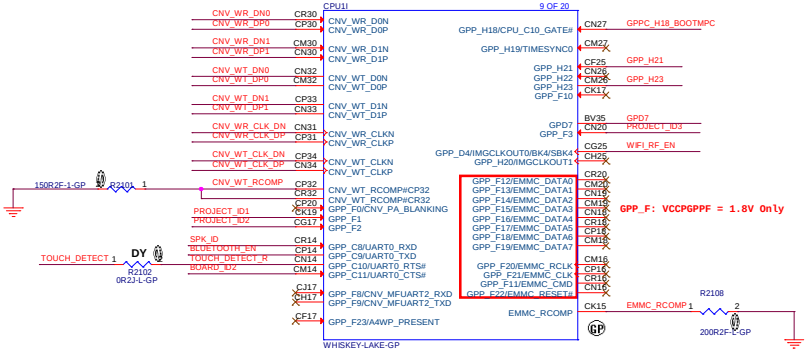
<Core Design>

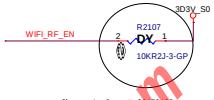
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

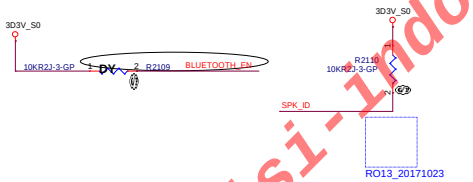
Title: CPU_(LPSS/ISH)
Size: A2 | Document Number: Jedi15"/17" WHL-U | Rev: A00
Date: Tuesday, January 08, 2019 | Sheet 20 of 106

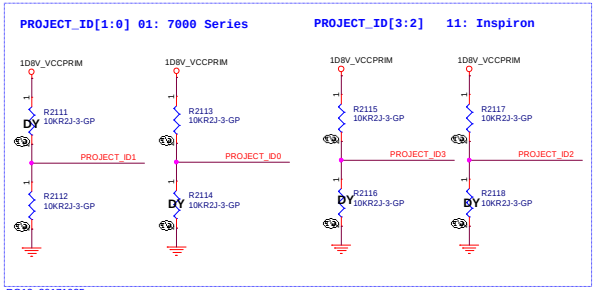
Main Func = PCH











Jedi UMA/DIS 2IN1

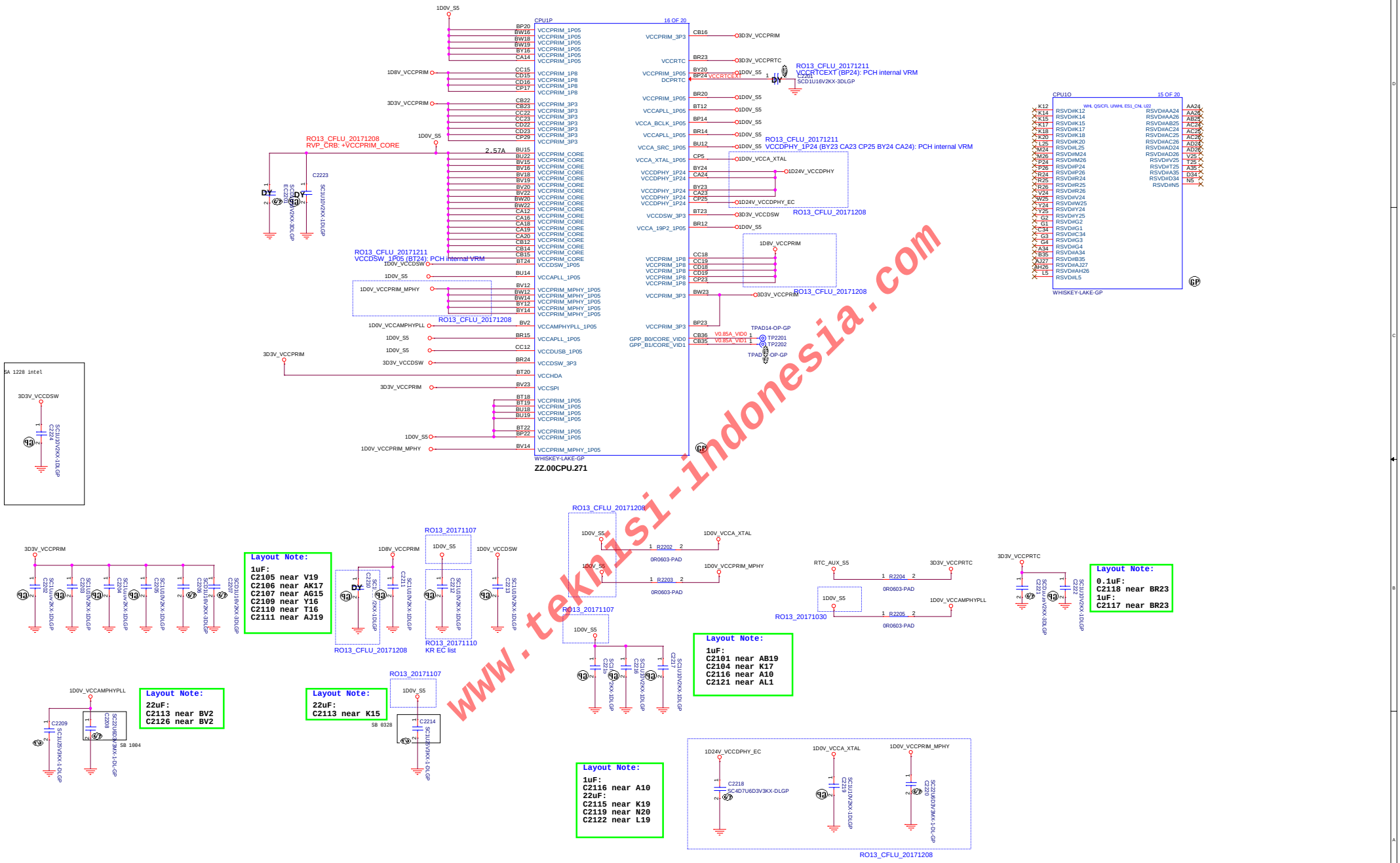
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (EMMC/CNVi)

Size: A2 | Document Number: Jedi15"/17" WHL-U | Rev: A00

Date: Tuesday, January 08, 2019 | Sheet 21 of 106

Main Func = PCH



Jedi UMA/DIS 2IN1

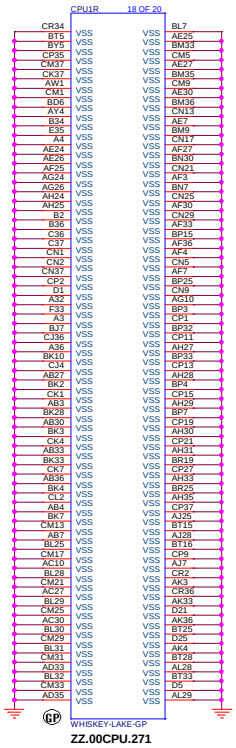
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

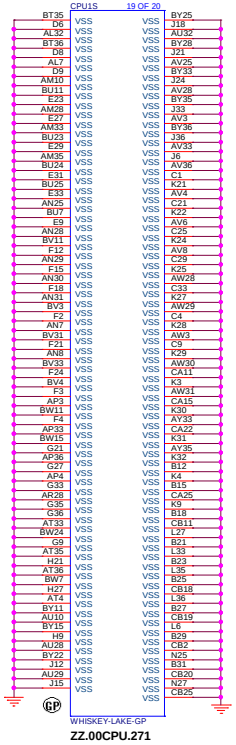
Title: CPU (PCH-LP PWR&Caps)

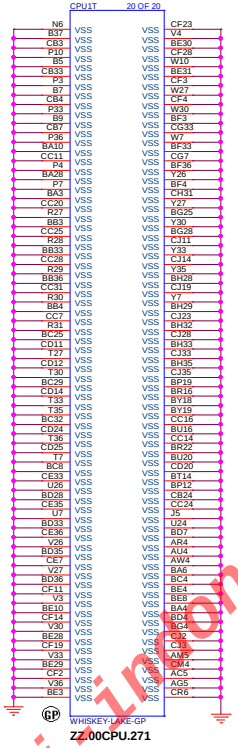
Size	Document Number	Rev
A2	Jedi15"/17" WHL-U	A00

Date: Tuesday, January 08, 2019 Sheet 22 of 106

Main Func = PCH







Skylake U Processor Corner NCTF Motherboard Test Point Example

Pin Number	Pin Name	Description	Corner
BB70	NCTFVSS	Test Point (TP)	Corner BB71
BB67	NCTFVSS	Test Point (TP)	
BA71	NCTFVSS	Test Point (TP)	
AV71	NCTFVSS	Test Point (TP)	
BA1	NCTFVSS	Test Point (TP)	Corner BB1
BA2	NCTFVSS	Test Point (TP)	
AV1	NCTFVSS	Test Point (TP)	
C1	NCTFVSS	Test Point (TP)	Corner A1
A5	NCTFVSS	Test Point (TP)	
A70	NCTFVSS	Test Point (TP)	Corner A71
A67	NCTFVSS	Test Point (TP)	
B71	NCTFVSS	Test Point (TP)	
E71	NCTFVSS	Test Point (TP)	

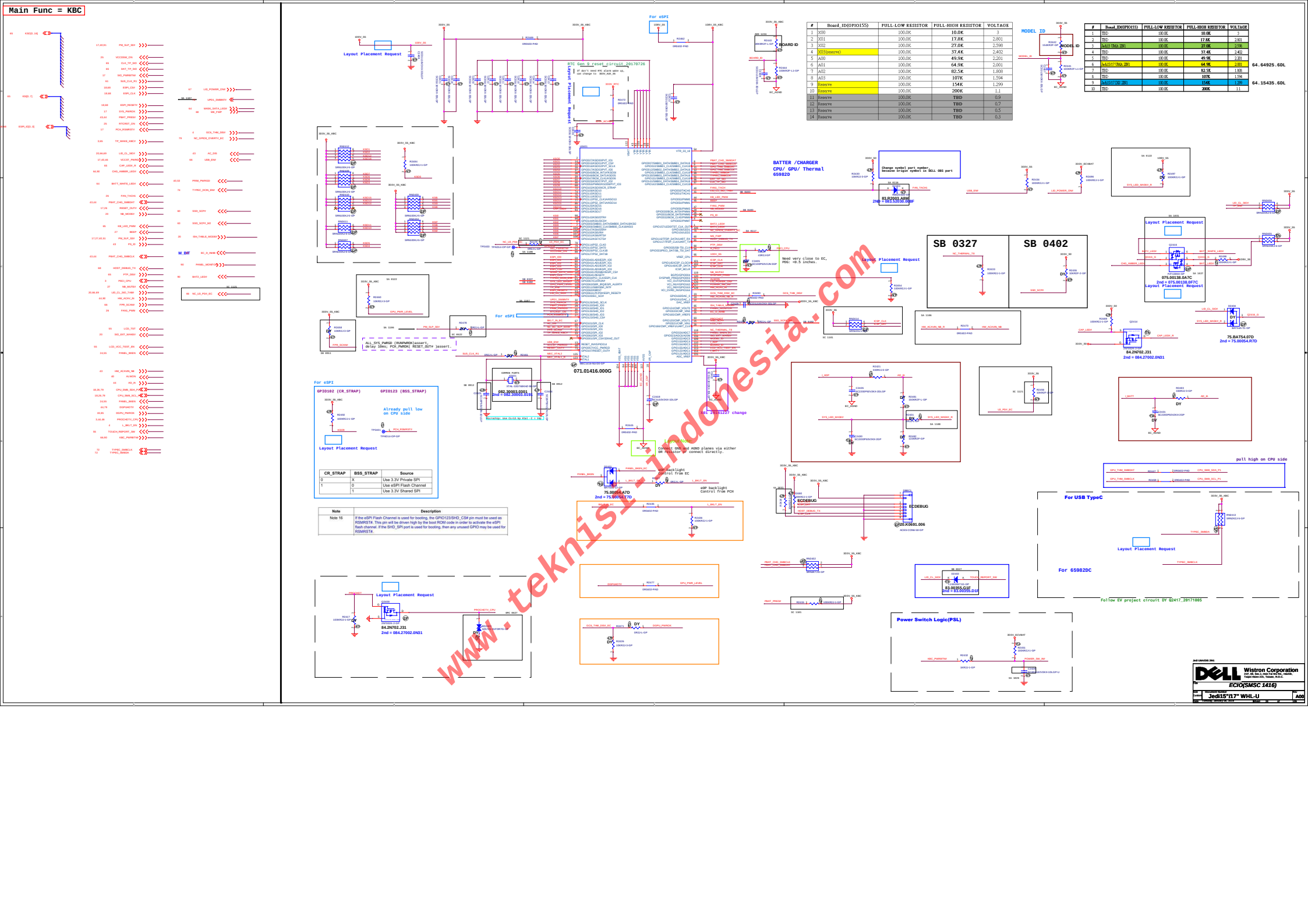
Jedi UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VSS)

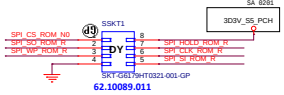
Size: A2 | Document Number: Jedi15"/17" WHL-U | Rev: A00

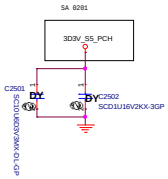
Date: Tuesday, January 08, 2019 | Sheet 23 of 106



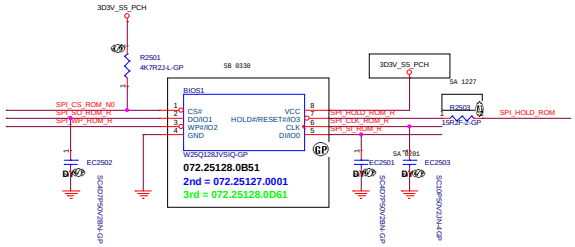
Main Func = SPI Flash

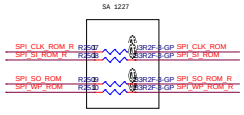
SPI Flash ROM(16M) for PCH



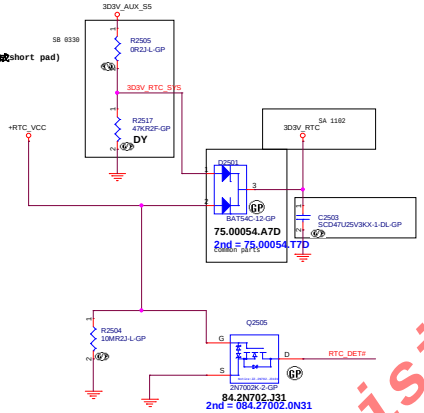


Source	QUAD/DUAL fast read	DUAL fast read	SFDP
072.25128.0B51	O	O	O
072.25127.0001	O	O	O
072.25128.0D61	O	O	O



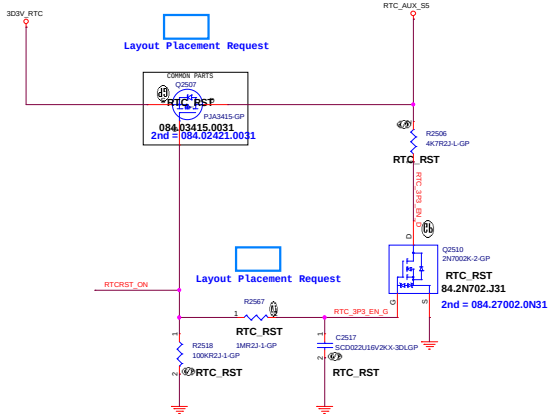


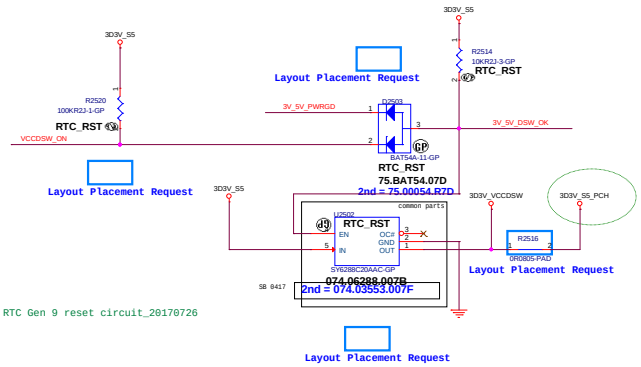
Main Func = RTC



29.2.1 VCCRTC External Circuit

On KBL, the VCCRTC max voltage is being reduced to minimize leakage on the ESD diodes and prevent RTC oscillator problems. Whether VCCRTC is sourced from Vbatt in G3 or VCCDSW_3p3 in Non-G3 state, platform designers must ensure the effective voltage at VCCRTC does not exceed 3.2V. The following sections will detail various options platform designers can use to achieve this new specification.



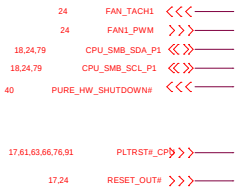


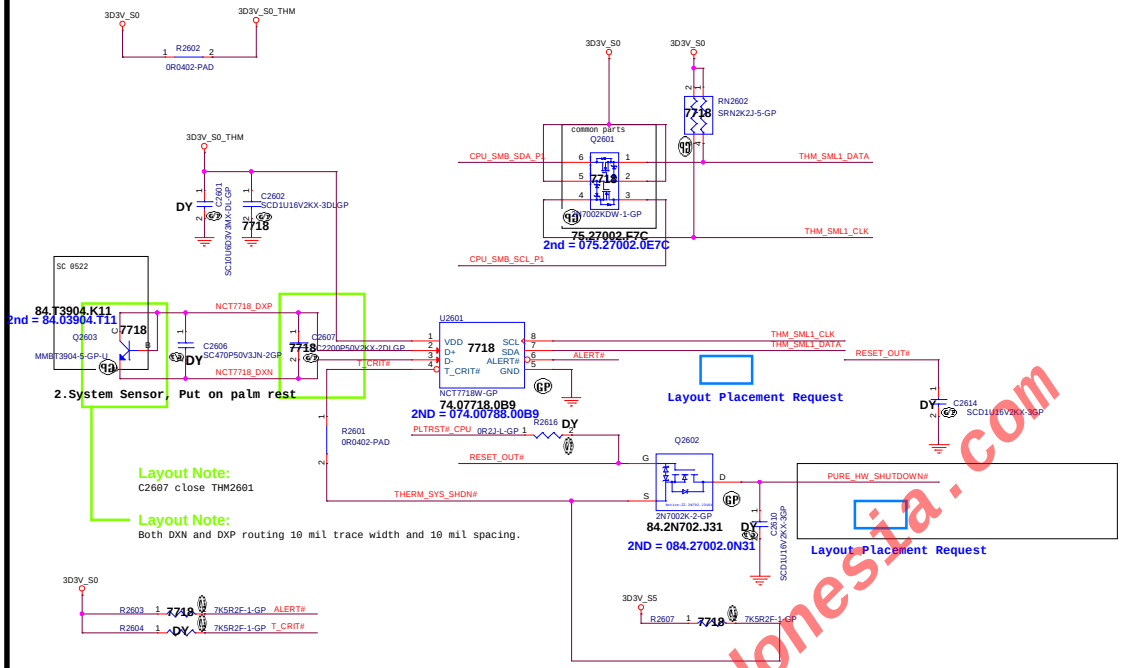
Jedi UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

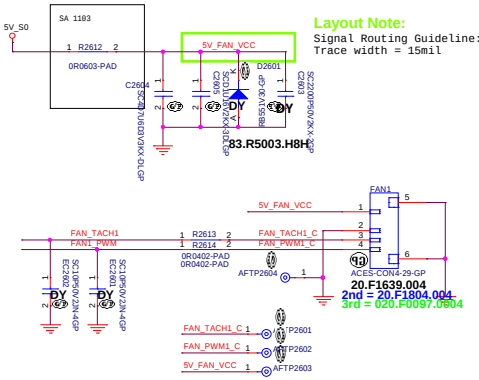
Title: Flash/RTC
Size: Custom | Document Number: Jedi15"/17" WHL-U | Rev: A00
Date: Tuesday, January 08, 2019 | Sheet 25 of 105

Main Func = Thermal Sensor





PWM FAN1



TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

Close to Thermal sensor

Layout Placement Request

Close to KBC
VD_IN1 for system thermal sensor

Layout Placement Request

Jedi UMA/DIS 2IN1

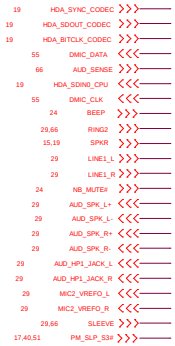
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

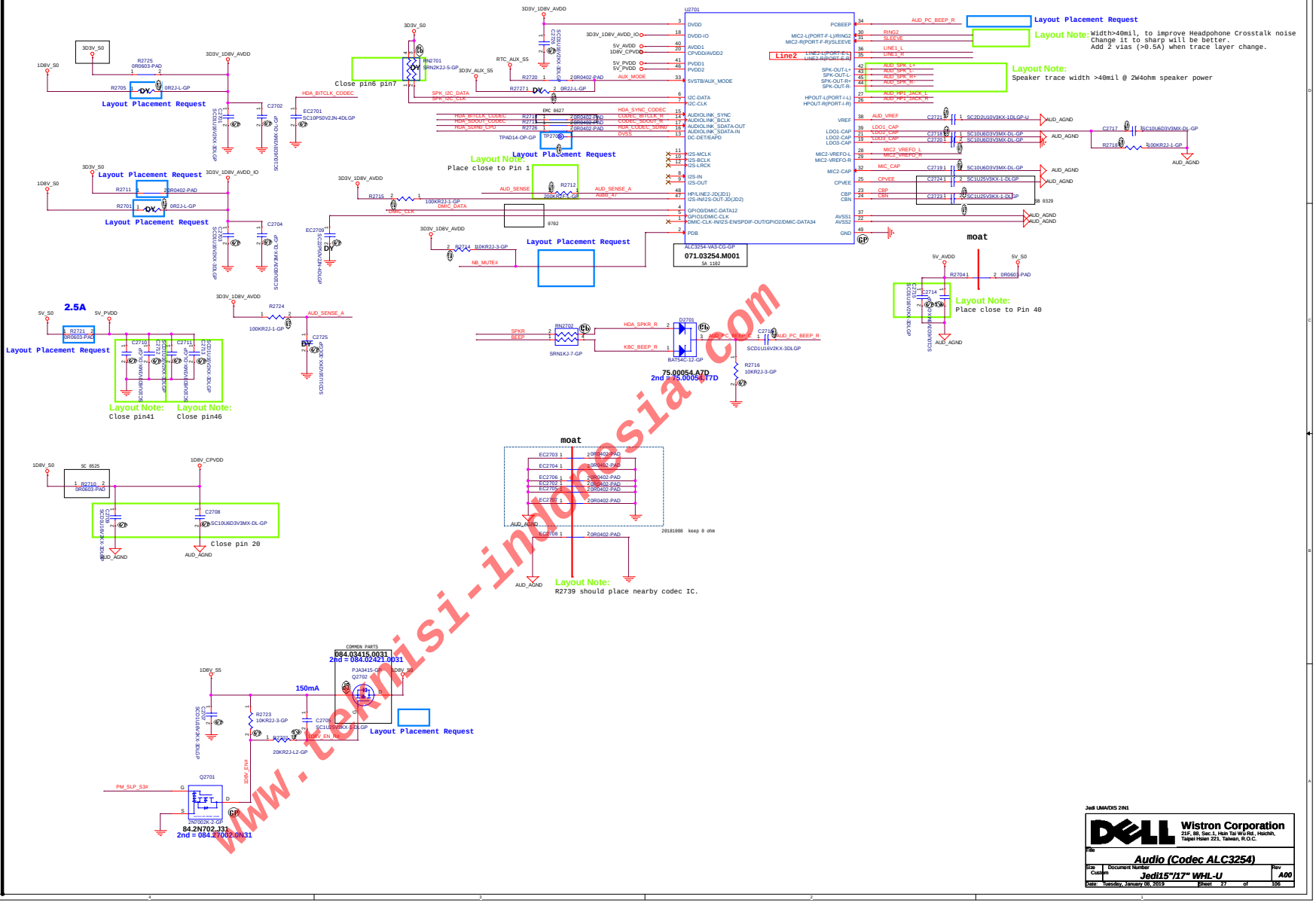
Title: INT IO (Thermal/Fan)

Size: A2 | Document Number: Jedi15"/17" WHL-U | Rev: A00

Date: Tuesday, January 08, 2019 | Sheet 26 of 106

Main Func = Audio





(Blanking)

Main Func = Audio

21 SPK_ID
27 AUD_SPK_L+
27 AUD_SPK_L-
27 AUD_SPK_R-
27 AUD_SPK_R+

27 MIC2_VREFO_R
27 MIC2_VREFO_L
27,66 RING2
27 LINE1_L

27 LINE1_R

27,66 SLEEVE

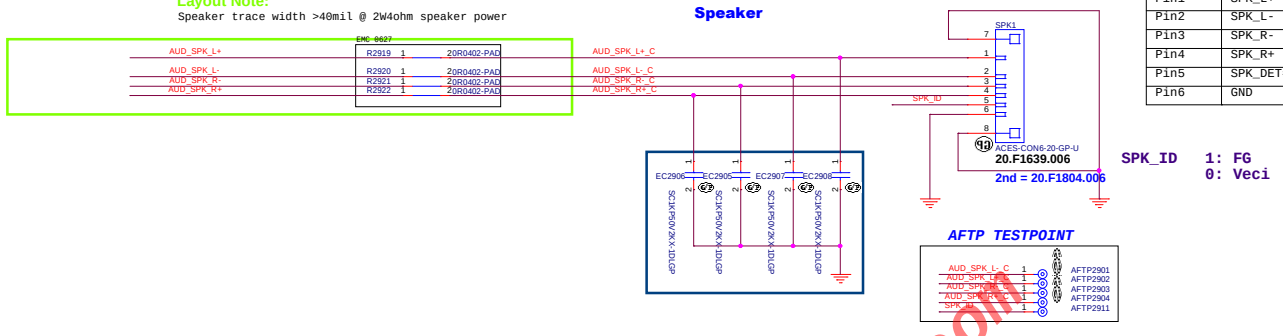
27 AUD_HP1_JACK_L
27 AUD_HP1_JACK_R

27,66 AUD_SENSE

66 AUD_HP1_JACK_L1
27,66 RING2_R
27,66 SLEEVE_R
66 AUD_HP1_JACK_R1

Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power

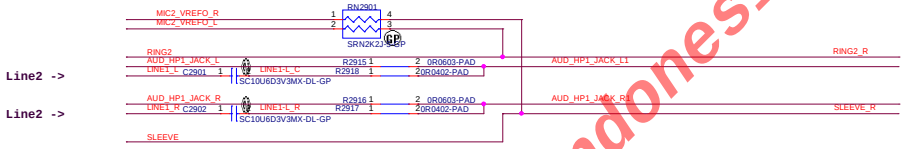
Speaker



CONN Pin	Net name
Pin1	SPK_L+
Pin2	SPK_L-
Pin3	SPK_R-
Pin4	SPK_R+
Pin5	SPK_DET#
Pin6	GND

SPK_ID 1: FG
0: Veci

AFTP TESTPOINT



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio IO
Size: A2
Document Number: Jedi15"/17" WHL-U
Rev: A00
Date: Tuesday, January 08, 2019
Sheet 29 of 106

Jedi UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Audio (RSVD)

Size	Document Number	Rev
A3	Jedi15"/17" WHL-U	A00

Date: Tuesday, January 08, 2019 Sheet 30 of 106

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Jedi UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN (RSVD)

Size	Document Number	Rev
A2	Jedi15"/17" WHL-U	A00

Date: Tuesday, January 08, 2019 Sheet 31 of 106

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Jedi UMA/DIS 2IN1

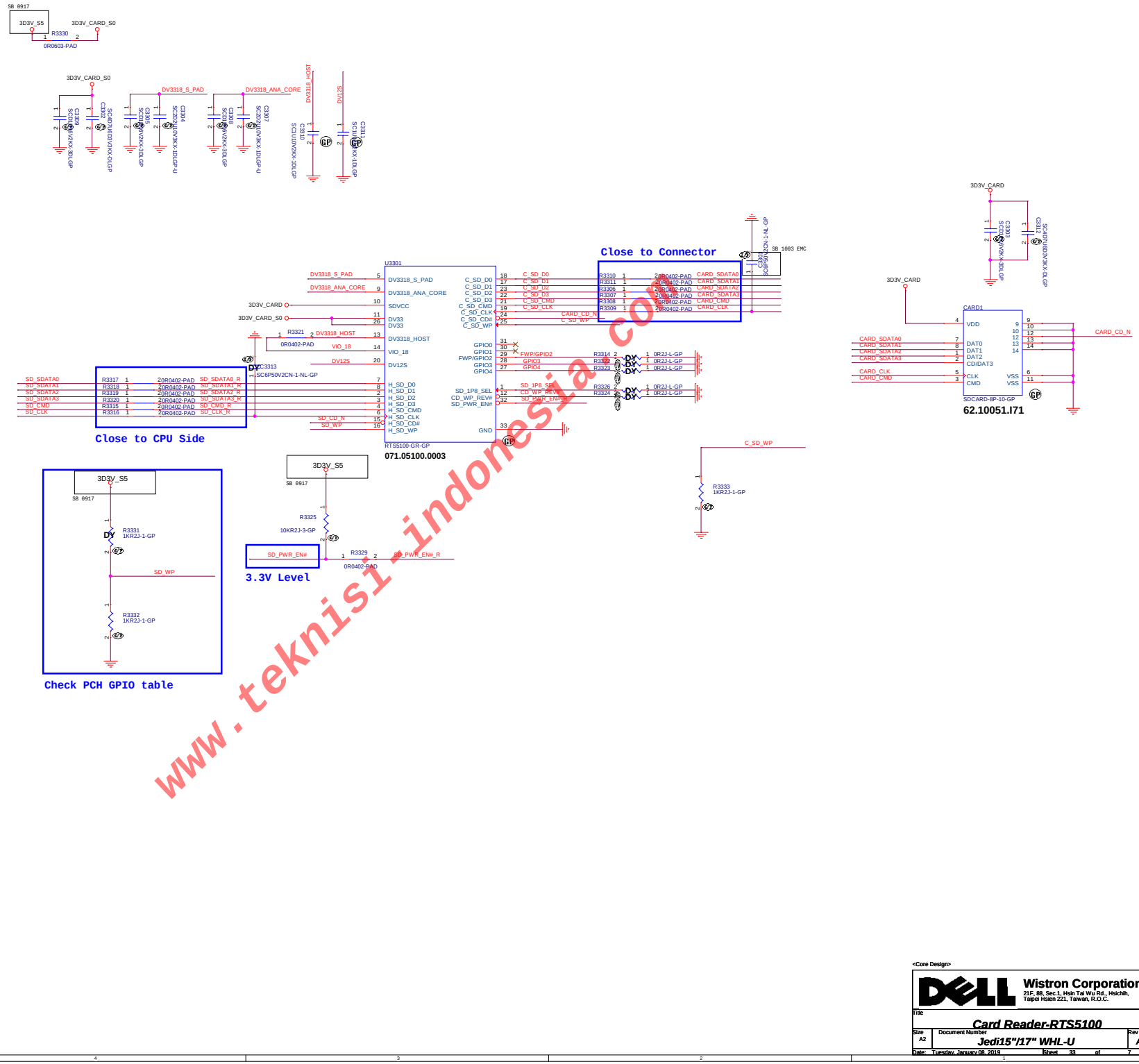
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN (RSVD) (RJ45+Transfor

Size	Document Number	Rev
A3	Jedi15"/17" WHL-U	A00

Date: Tuesday, January 08, 2019 Sheet 32 of 106

Main Func = Card Reader



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Card Reader-RTS5100

Size	Document Number	Rev
A2	Jedi15"/17" WHL-U	A00

Date: Tuesday, January 08, 2019 Sheet 33 of 7

Jedi UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

USB (RSVD) (USB2.0 CONN)

Size	Document Number	Rev
A3	Jedi15"/17" WHL-U	A00

Date: Tuesday, January 08, 2019 Sheet 34 of 106

Jedi UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

USB (RSVD) (USB3.0 Conn)

Size	Document Number	Rev
	Jedi15"/17" WHL-U	A00

Date: Tuesday, January 08, 2019 Sheet 35 of 106

Jedi UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

USB (RSVD) (USB Charger)

Size	Document Number	Rev
A3	Jedi15"/17" WHL-U	A00

Date: Tuesday, January 08, 2019 Sheet 36 of 106

Jedi UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

USB (RSVD) (PCIE to USB3.0)

Size	Document Number	Rev
A4	Jedi15"/17" WHL-U	A00

Date: Tuesday, January 08, 2019 Sheet 37 of 106

Jedi UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

USB (RSVD) (USB3.0 Redriver)

Size	Document Number	Rev
A4	Jedi15"/17" WHL-U	A00

Date: Tuesday, January 08, 2019 Sheet 38 of 106

Jedi UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Sequence (RSVD)

Size	Document Number	Rev
A2	Jedi15"/17" WHL-U	A00

Date: Tuesday, January 08, 2019 Sheet 39 of 106

Main Func = Power Plane & Sequence

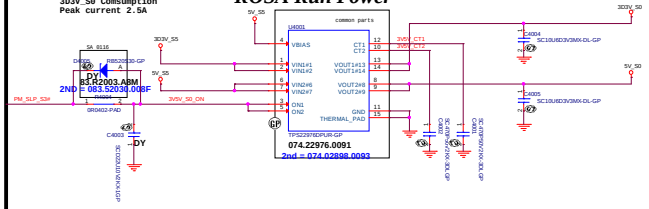
5V_S0

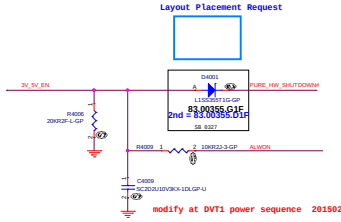
5V_S0 Comsumption
Peak current 5A

3D3V_S0

3D3V_S0 Comsumption
Peak current 2.5A

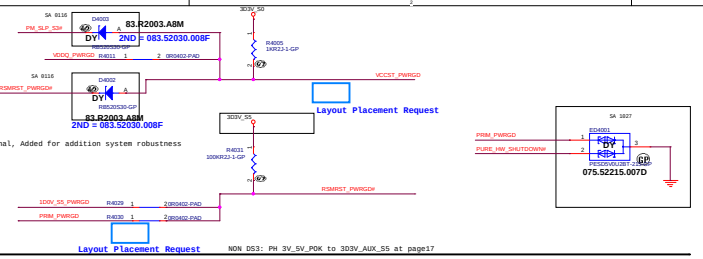
ROSA Run Power





modify at DVT1 power sequence 20150203

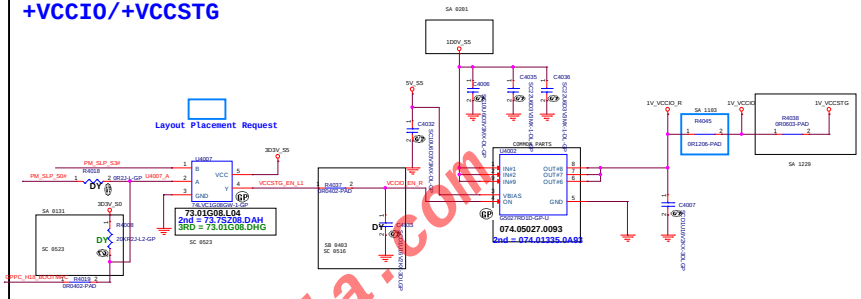
Power Good



[#543016] Optional, Added for addition system robustness

NON DS3: PH 3V_5V_POK to 3D3V_AUX_S5 at page17

+VCCIO/+VCCSTG



EOPIO and EDRAM

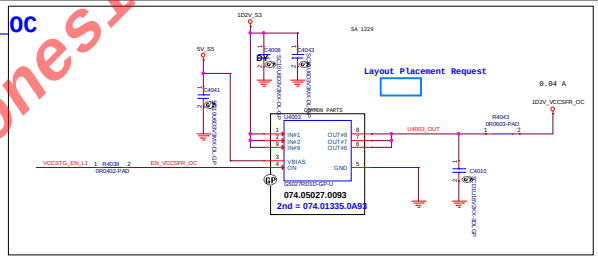
+V_EDRAM_VR

Voltage = 1.0 V ± 50 mV
Imax = 3.2 A
TRISE = 240 us

+V_EOPIO_VR

Voltage = 1.0 V ± 50 mV
Imax = 2.8 A
TRISE = 240 us

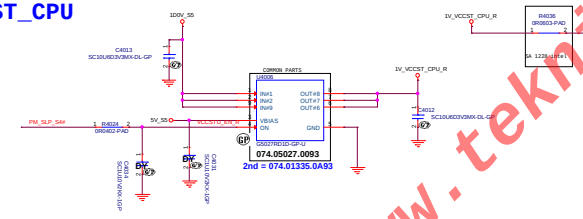
1D2V_VCCSFR_OC



VCCST, VCCSTG, and VCCPLL can remain powered during S4 and S5 power states for board VR optimization.

MANAGEMENT RAIL POWER GENERATION

VCCST_CPU



+V1.8S0

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Sequence (Power Enable)

Jedi15"/17" WHL-U

A00

Jedi UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Sequence (RSVD) (DS3/S0ix)

Size	Document Number	Rev
A4	Jedi15"/17" WHL-U	A00

Date: Tuesday, January 08, 2019 Sheet 41 of 106

Jedi UMA/DIS 2IN1

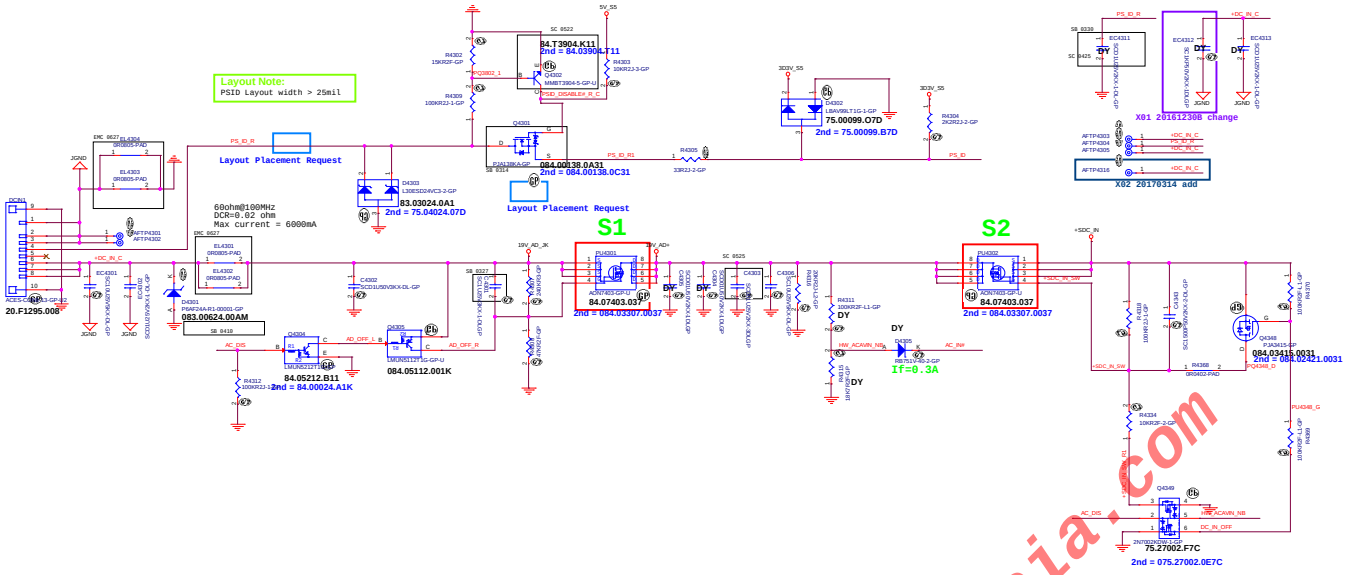
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (RSVD)

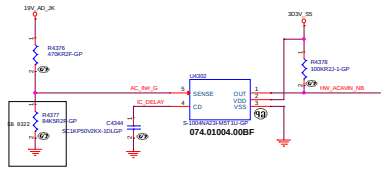
Size: A2 | Document Number: Jedi15"/17" WHL-U | Rev: A00

Date: Tuesday, January 08, 2019 | Sheet 42 of 106

Main Func = ADT Input

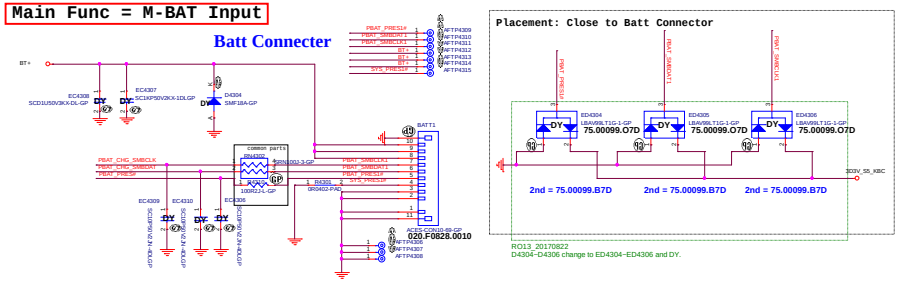


Barrel Adapter Piug-in Detect



Main Func = M-BAT Input

Batt Connecter



Jedi UMA/DIS 28N1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

File: INT IO (ATX/ DC/ BATT Conn)

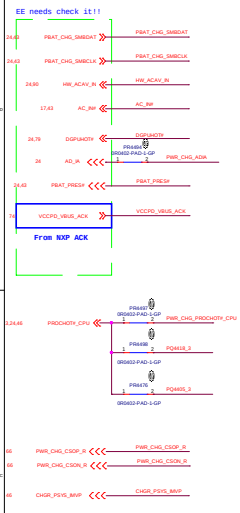
Size	Document Number	Rev
A1	Jedi15"/17" WHL-U	A00

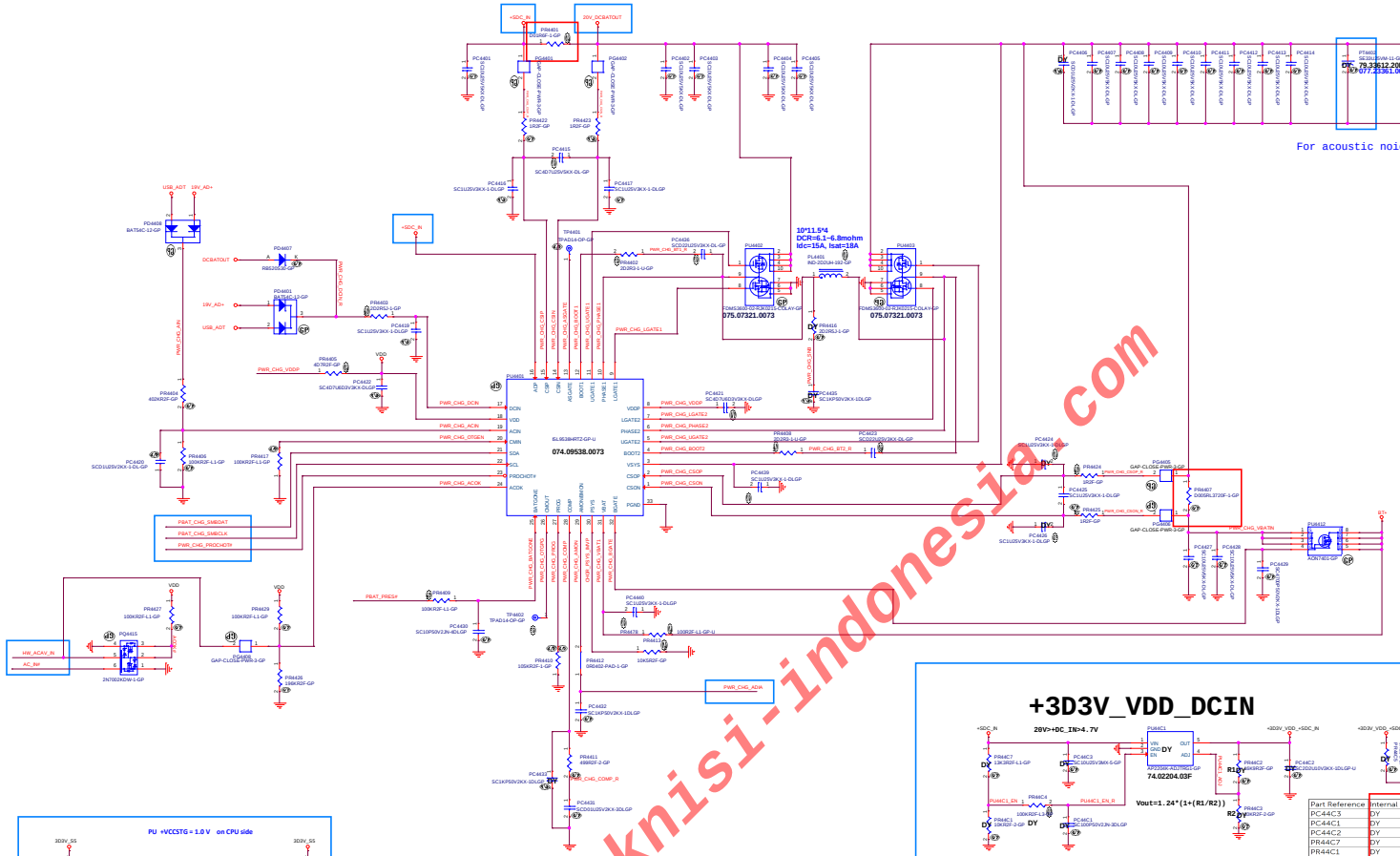
Date: Tuesday, January 08, 2013 Sheet 43 of 106

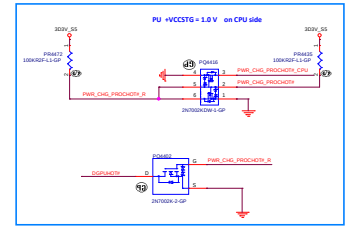
ISL9538H For Charger

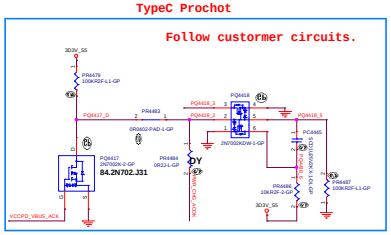
Main Func = Charger

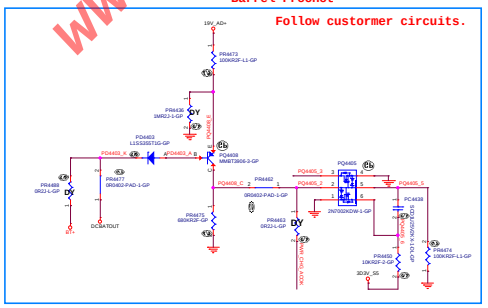
OFFPAGE

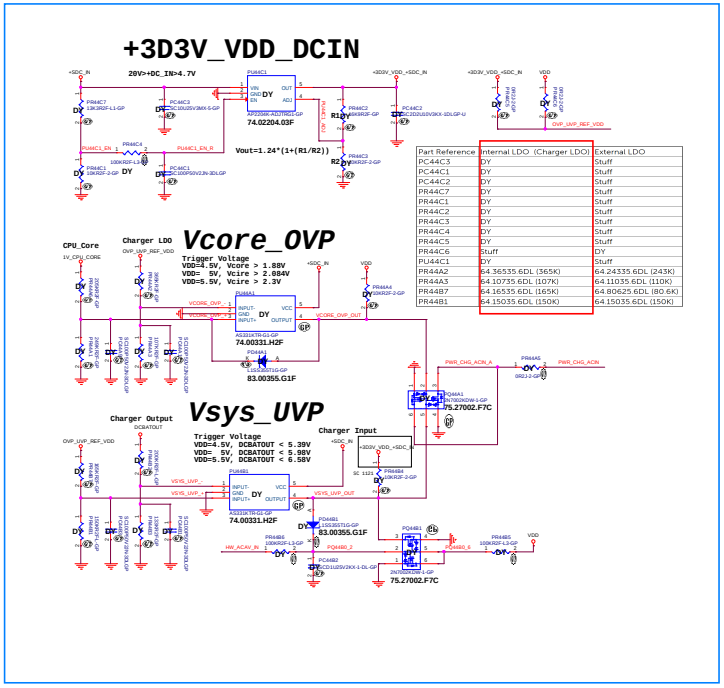












Part Reference	Internal LDO (Charger LDO)	External LDO
PC44C3	DY	Stuff
PC44C1	DY	Stuff
PC44C2	DY	Stuff
PR44C7	DY	Stuff
PR44C1	DY	Stuff
PR44C2	DY	Stuff
PR44C3	DY	Stuff
PR44C4	DY	Stuff
PR44C5	DY	Stuff
PR44C6	Stuff	DY
PU44C1	DY	Stuff
PR44A2	64.36535.6DL (365K)	64.24335.6DL (243K)
PR44A3	64.10735.6DL (107K)	64.11035.6DL (110K)
PR44B7	64.16535.6DL (165K)	64.80625.6DL (80.6K)
PR44B1	64.15035.6DL (150K)	64.15035.6DL (150K)

TABLE 22. PROG PIN PROGRAMMING OPTIONS

PROG-GND RESISTANCE (kΩ) MIN	TYP 1%	MAX	CELL #	DEFAULT SWITCHING FREQUENCY	Autonomous charging	DEFAULT ACLimit1 Reg(A)
0			1	733kHz	No	0.476
8.45				733kHz	No	1.5
14.7				1MHz	No	1.5
21.0				1MHz	No	0.476
28.0				733kHz	Yes	0.476
35.7				733kHz	Yes	1.5
43.2			2	733kHz	Yes	1.5
52.3				733kHz	Yes	0.476
61.9				1MHz	No	0.476
71.5				1MHz	No	1.5
82.5				733kHz	No	1.5
93.1				733kHz	No	0.476
105			3	733kHz	No	0.476
118				733kHz	No	1.5
133				1MHz	No	1.5
147				1MHz	No	0.476
162				733kHz	Yes	0.476
178				733kHz	Yes	1.5
196			4	733kHz	Yes	1.5
215				733kHz	Yes	0.476
237				1MHz	No	0.476
261				1MHz	No	1.5
287				733kHz	No	1.5
316				733kHz	No	0.476
348			1	733kHz	No	0.476

Wistron Corporation
Power (Charger_ISL9538)
Size: Custom | Document Number: STD | Rev: A00
Date: Tuesday, January 08, 2019 | Sheet 44 of 55

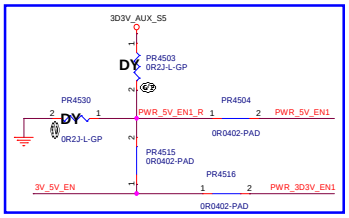
Main Func = PWR.Plane.Regulator_5V

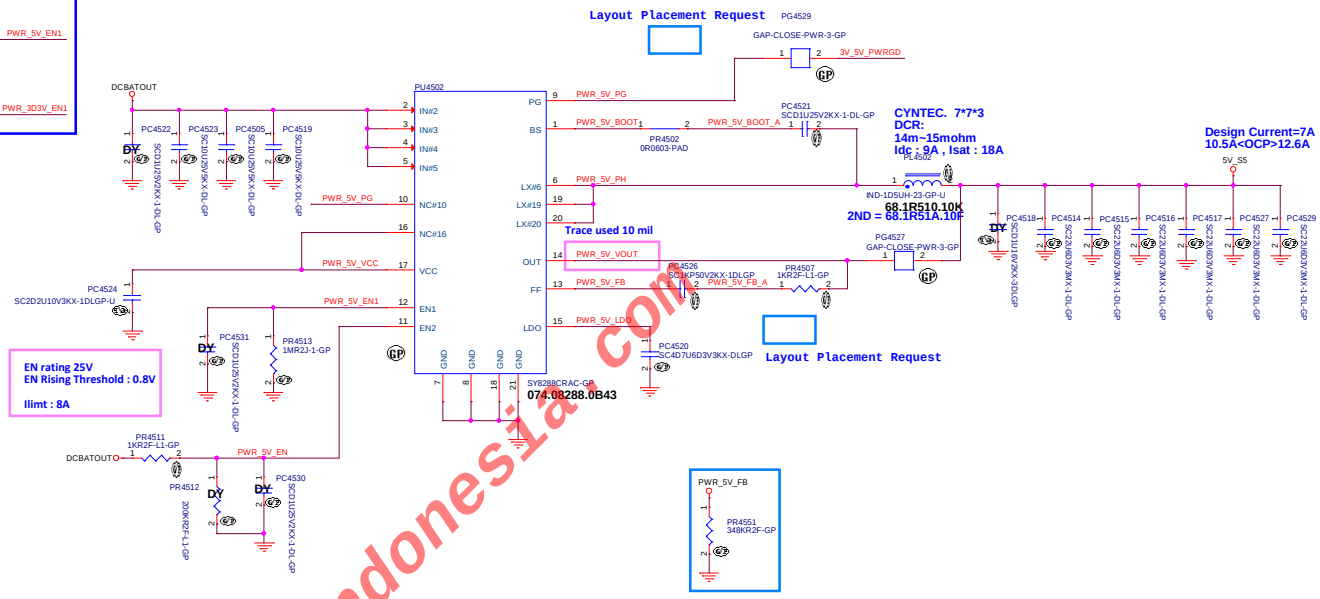
OFFPAGE-Signal

40 3V_5V_EN

17,25,45 3V_5V_PWRGD

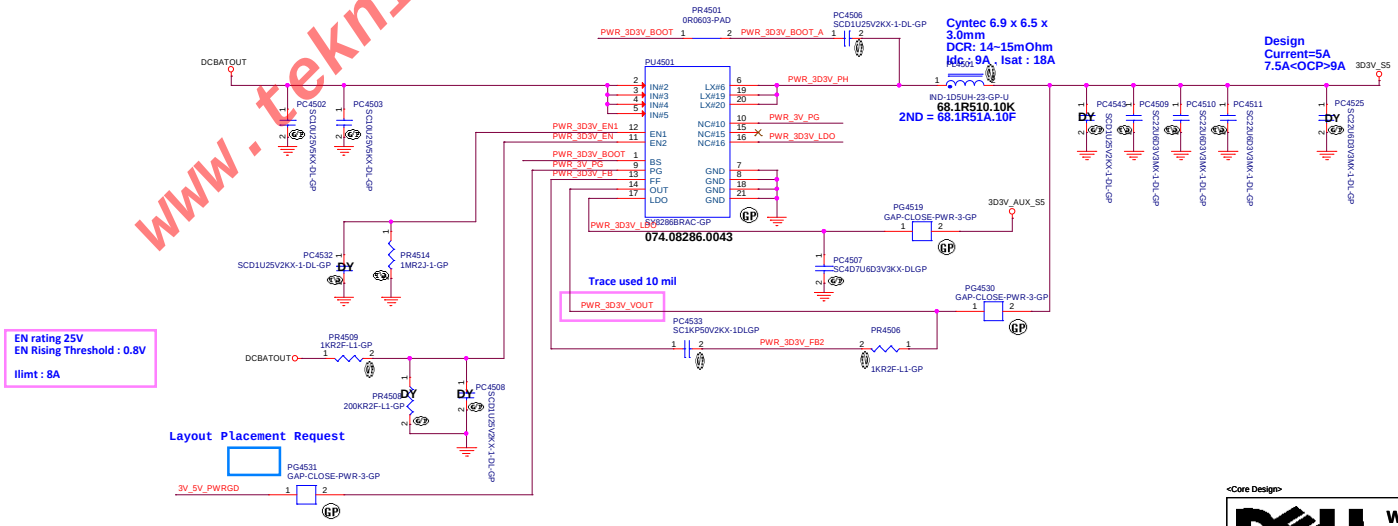
OFFPAGE-GAP





Main Func = PWR.Plane.Regulator_3D3V

17,25,45 3V_5V_PWRGD



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

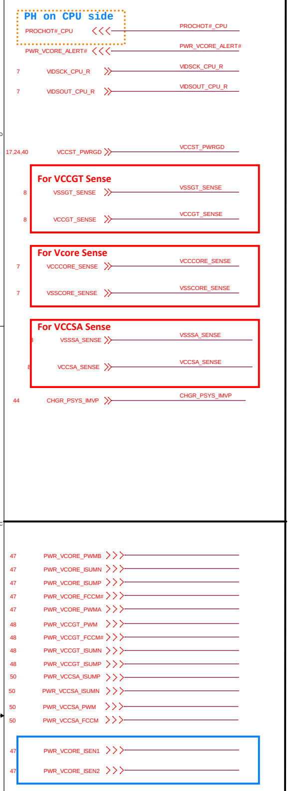
Title: Power (SY8288/8286_5V/3D3V)

Size: A2 | Document Number: Jedi15"/17" WHL-U | Rev: A00

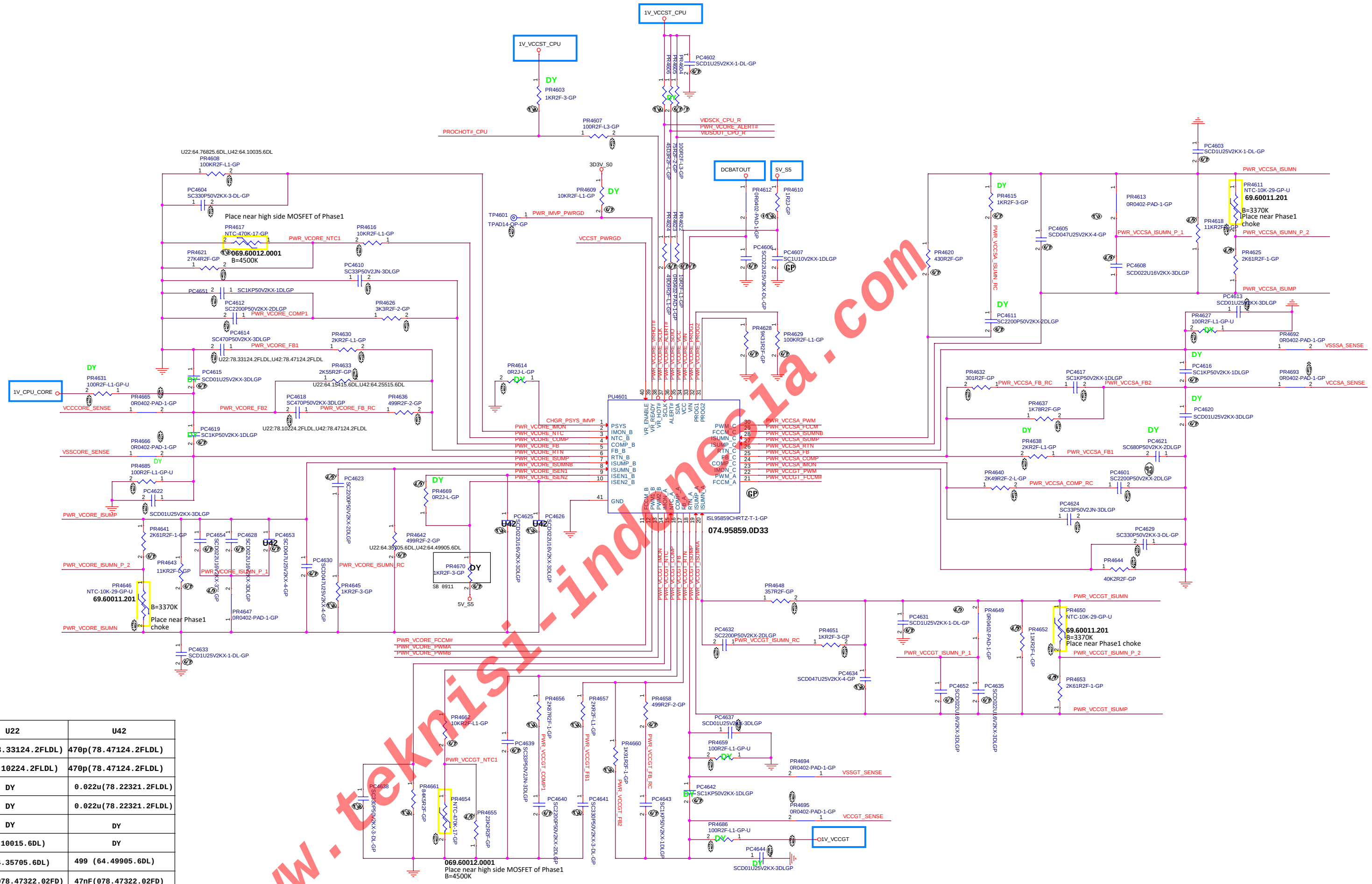
Date: Tuesday, January 08, 2019 | Sheet 45 of 106

Main Func = CPU_CORE

OFFPAGE



ISL95859C For CPUCORE



	U22	U42
PC4614	330P(78.33124.2FLDL)	470p(78.47124.2FLDL)
PC4618	1KP(78.10224.2FLDL)	470p(78.47124.2FLDL)
PC4625	DY	0.022u(78.22321.2FLDL)
PC4626	DY	0.022u(78.22321.2FLDL)
PR4669	DY	DY
PR4635	1K(64.10015.6DL)	DY
PR4642	357(64.35705.6DL)	499 (64.49905.6DL)
PC4630	47nF(078.47322.02FD)	47nF(078.47322.02FD)
PC4628	22nF(78.22321.2FLDL)	22nF(78.22321.2FLDL)
PC4654	10nF(78.10324.2FLDL)	22nF(78.22321.2FLDL)
PC4653	DY	47nF(078.47322.02FD)
PR4633	1.54K(64.15415.6DL)	2.55K(64.25515.6DL)
PR4608	76.8K(64.76825.6DL)	100K (64.10035.6DL)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (95859_CPUCORE(1/3))

Size: A1 | Document Number: STD | Rev: A00

Main Func = CPU_CORE

AOZ5038Q For VCORE

OFFPAGE

DCBATOUT

PWR_DCBATOUT_VCOREA

PL4703 HCB2012KF-800T50-GP-U 68.00216.191

PL4704 HCB2012KF-800T50-GP-U 68.00216.191

G4701 0R1206-PAD

A00 1224

PWR_VCORE_PWMA
PWR_VCORE_FCCM#
PWR_VCORE_ISEN1
PWR_VCORE_ISUMP
PWR_VCORE_ISUMN
PWR_VCORE_ISEN2

PWR_VCORE_PWMB
PWR_VCORE_FCCM#
PWR_VCORE_ISEN2
PWR_VCORE_ISUMP
PWR_VCORE_ISUMN
PWR_VCORE_ISEN1

PWR_DCBATOUT_VCOREA

PC4702 PC4703 PC4704 PC4705 SC10U25V3MX-6-GP

For acoustic noise

PWR_DCBATOUT_VCOREA

PT4702 SE33U25VM-11-GP 79.23612.20L 077.23361.0001

PC4714 PC4715 PC4716 PC4717 SC10U25V3MX-6-GP

5V_S5

PR4703 2D2R2F-GP

PC4777 SC2D2U6D3V2MX-DL-GP

PC4709 SC2D2U6D3V2MX-DL-GP

PWR_VCORE_VCCDA

PR4702 0R0402-PAD-1-GP

PR4717 5K11R2F-L1-GP

PR4706 0R0402-PAD-1-GP

PU4701 AOZ5038QI-05-GP 074.05038.0A73

PWR_VCORE_PWMA_RA

PWR_VCORE_FCCM#_RA

PWR_DCBATOUT_VCOREA

PWR_VCORE_BOOTA

PWR_VCORE_BOOTRA

PWR_VCORE_SWA

PWR_VCORE_BOOTA_RC

PR4704 2D2R3-1-U-GP

PC4708 SCD22U25V3KX-DL-GP

Cyntec 6.8mmx7.6mmx3.0mm
DCR: 0.9m ohm +/-7%
Idc : 38A , Isat : 45A

WHL_U42_15W
Icc(max)=71A
TDC=48A

1V_CPU_CORE

PL4701 IND-D15UH-33-GP

068.R1510.1171
2nd = 068.R1510.1141

PT4701 SE330U2VDM-4-GP 79.33719.20C

PR4705 2D2R6J-3-GP

PWR_VCORE_SNB1

PC4710 SC1KP50V2KX-1DLGP

PG4708 GAP-CLOSE-PWR-3-GP

PG4709 GAP-CLOSE-PWR-3-GP

PWR_VCORE_ISUMN_GA

PWR_VCORE_ISEN1

PWR_VCORE_ISUMP

PWR_VCORE_ISUMN

PWR_VCORE_ISEN2

PR4721 100KR2F-L1-GP

PR4708 3K65R2F-1-GP

PR4709 10R2F-L1-GP

PR4722 100KR2F-L1-GP

PWR_DCBATOUT_VCOREA

PC4712 SC2D2U6D3V2MX-DL-GP

PR4713 2D2R2F-GP

PC4766 SC2D2U6D3V2MX-DL-GP

PWR_VCORE_VCCDB

PR4711 0R0402-PAD-1-GP

PR4718 5K11R2F-L1-GP

PR4712 0R0402-PAD-1-GP

PWR_VCORE_PWMB_RA

PWR_VCORE_FCCM#_RB

PU4702 AOZ5038QI-05-GP 074.05038.0A73

PWR_DCBATOUT_VCOREA

PWR_VCORE_BOOTB

PWR_VCORE_BOOTRB

PWR_VCORE_SWB

PWR_VCORE_BOOTB_RC

PR4710 2D2R3-1-U-GP

PC4711 SCD22U25V3KX-DL-GP

Cyntec 6.8mmx7.6mmx3.0mm
DCR: 0.9m ohm +/-7%
Idc : 38A , Isat : 45A

1V_CPU_CORE

PL4702 IND-D15UH-33-GP

068.R1510.1171
2nd = 068.R1510.1141

PT4703 SE330U2VDM-4-GP 79.33719.20C

PR4714 2D2R6J-3-GP

PWR_VCORE_SNB2

PC4713 SC1KP50V2KX-1DLGP

PG4713 GAP-CLOSE-PWR-3-GP

PG4715 GAP-CLOSE-PWR-3-GP

PWR_VCORE_ISUMN_GB

PWR_VCORE_ISEN2

PWR_VCORE_ISUMP

PWR_VCORE_ISUMN

PWR_VCORE_ISEN1

PR4723 100KR2F-L1-GP

PR4716 3K65R2F-1-GP

PR4715 10R2F-L1-GP

PR4724 100KR2F-L1-GP

Wistron Corporation
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Title: POWER (5038_CPU_VCORE(2/3))

Size: A2 | Document Number: STD | Rev: A00

Date: Wednesday, January 09, 2019 | Sheet 47 of 106

Main Func = CPU_CORE

Offpage-Signal

AOZ5038Q For VCCGT

DCBATOUT PWR_DCBATOUT_VCCGT

PL4802 HCB2012KF-800T50-GP-U 68.00216.191

PL4803 HCB2012KF-800T50-GP-U 68.00216.191

46 PWR_VCCGT_PWM
PWR_VCCGT_FCCM#
46 PWR_VCCGT_ISUMP
46 PWR_VCCGT_ISUMN

PWR_DCBATOUT_VCCGT

PC4801 SC10U25V3MX-5-GP DY
PC4802 SC10U25V3MX-5-GP
PC4803 SC10U25V3MX-5-GP
PC4804 SC10U25V3MX-5-GP

For acoustic noice

PWR_DCBATOUT_VCCGT

PT4805 SE33U25VM-11-GP
79.33612.20L
077.23361.0001

5V_S5

PC4866 SC2D2U6D3V2MX-DL-GP

PR4804 2D2R2F-GP

PWR_VCCGT_VCC_R

PC4808 SC2D2U6D3V2MX-DL-GP

PR4802 0R0402-PAD-1-GP

PWR_VCCGT_PWM

PR4812 5K11R2F-L1-GP DY

PR4806 0R0402-PAD-1-GP

PWR_VCCGT_FCCM#

PWR_VCCGT_PWM_R

PWR_VCCGT_FCCM#_R

PU4801

AOZ5038QI-05-GP
074.05038.0A73

NC#31 PWM FCCM NC#30 NC#6 GL#27 GL#35
VCC PVCC VIN VIN VIN VIN VIN
BOOT VSWH#7
VSWH#16 VSWH#17 VSWH#18 VSWH#19 VSWH#20 VSWH#21 VSWH#22 VSWH#23 VSWH#24 VSWH#25 VSWH#26
NC#4 AGND PGND PGND PGND PGND PGND

PWR_DCBATOUT_VCCGT

PWR_VCCGT_BOOT_RC

PR4805 2D2R3F-L-GP

PC4807 SCD22U25V3KX-DL-GP

PWR_VCCGT_BOOT
PWR_VCCGT_BOOTR

PWR_VCCGT_SW

Cyntec 6.8mmx7.6mmx3.0mm
DCR: 0.9m ohm +/-7%
Idc : 38A , Isat : 45A

WHL_U42_15W
Icc(max)=31A
TDC=18A

PL4801 IND-D15UH-33-GP
068.R1510.1171
2nd = 068.R1510.1141

1V_VCCGT

PR4803 2D2R6J-3-GP DY

PWR_VCCGT_SNB

PC4806 SC1KP50V2KX-1DLGP DY

PG4807 GAP-CLOSE-PWR-3-GP

PG4808 GAP-CLOSE-PWR-3-GP

PT4801 SE330U2VDM-4-GP
PANASONIC
ESR: 9 mohm

PWR_VCCGT_ISUMP_G

PWR_VCCGT_ISUMN_G

PR4808 3K65R2F-1-GP

PR4801 0R0402-PAD-1-GP

PWR_VCCGT_ISUMP

PWR_VCCGT_ISUMN

Wistron Corporation
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Title: POWER (5038_CPU_VCORE(3/3))

Size: A3 | Document Number: STD | Rev: A00

Date: Tuesday, January 08, 2019 | Sheet 48 of 106

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NCP81210MN_CPU_VCCGTUS

Size: A2 | Document Number: Jedi15"/17" WHL-U | Rev: A00

Date: Tuesday, January 08, 2019 | Sheet 49 of 106

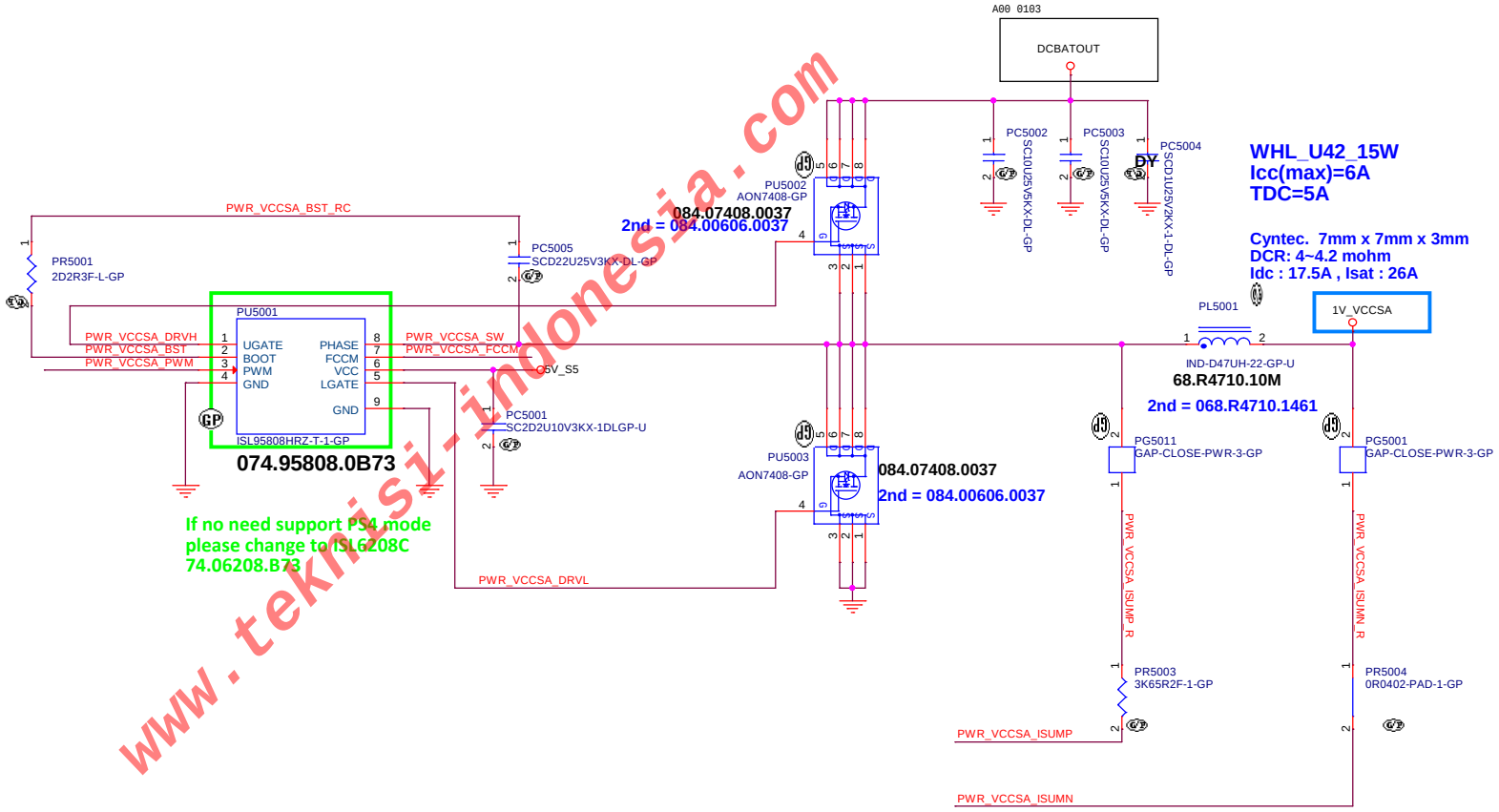
Main Func = CPU_CORE

OFFPAGE-Signal

- PWR_VCCSA_PWM
- PWR_VCCSA_ISUMP
- PWR_VCCSA_ISUMN
- PWR_VCCSA_FCCM

OFFPAGE-GAP

A00 0103



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VCCSA

Size	Document Number	Rev
A3	Jedi15"/17" WHL-U	A00

Date: Wednesday, January 09, 2019 Sheet 50 of 106

Main Func = PWR.Plane.Regulator_1D2V/0D6V

OFFPAGE-Signal

40 VDDQ_PWRGD
EE needs check it!!

51 PWR_2D5V_PG
EE needs check it!!

17,27,40 PM_SLP_S3#

5 SM_PGCNTL_R

51 PWR_2D5V_PG

17,40,66 PM_SLP_S4#

OFFPAGE-GAP

A00 0103

5V_S5 PR5108 10R2J-L-GP PWR_VDDQ_VCC PC5108 SC22U6D3V2MX-DL-GP
PC5112 SC4D7U6D3V3KX-L-GP DY
If 5V has droop Please mount it
PR5102 6K49R2F-1-GP PWR_VDDQ_CS
DCBATOUT A00 0103
PC5116 SCD1U25V2KX-1-DL-GP DY
PC5111 SC10U25V5KX-DL-GP
PC5115 SC10U25V5KX-DL-GP
PD5101 AZ4024-01L-R7G-GP
DY 083.04024.0AA1

3D3V_S5 PR5104 100KR2J-1-GP DY
PR5103 = 510K
Fs = 400~550KHz
PG5114 GAP-CLOSE-PWR-3-GP VDDQ_PWRGD
DCBATOUT A00 0103
PR5103 510KR2F-GP
PG5110 GAP-CLOSE-PWR-3-GP 1D2V_S3
PG5116 GAP-CLOSE-PWR-3-GP
PC5122 SC1U10V2KX-1DLGP
Design Current = 700mA
0D6V_S0
PC5117 SCD1U25V2KX-1-DL-GP DY
PC5124 SC10U6D3V3MX-DL-GP

PU5101 G5388K11U-GP 074.05388.0043
CS VCC PGOOD TON S5 S3 VLDOIN VTTGND VTTGND VTTGND VTT VTTSNS NC/FB GND BST LX#25 LX#17 LX#18 LX#19 LX#20 LX#35 PGND PGND PGND PGND PGND PGND VDDQSNS VDDQSET VTTREF
PWR_VDDQ_PG PWR_VDDQ_TON PWR_VDDQ_EN PWR_VTT_EN PWR_VDDQ_VLDOIN PWR_VDDQ_BOOT PWR_VDDQ_BOOTA PWR_VDDQ_BOOTB PWR_VDDQ_PH PWR_VDDQ_VDDQ PWR_VDDQ_FB PWR_VDDQ_VTTREF
PR5111 0R0603-PAD PC5114 SCD1U25V2KX-1-DL-GP

PL5101 IND-D68UH-40-GP
Cyntec. 5 x 5 x 3.0 mm
DCR: 11m~12mOhm
Idc : 8.5A , Isat : 14A
68.R6810.20E
2nd = 68.R681B.10A
Design Current=6A
7.8A < OCP < 10.4A
PG5113 GAP-CLOSE-PWR-3-GP
PC5109 PC5105 PC5104 PC5107 SC22U6D3V3MX-1-DL-GP
1D2V_S3
R1 PR5107 6K2R2F-GP
R2 PR5101 10K2R2F-GP
Vo=0.75x(1+R1/R2)
=0.75x(1+6.2/10)
=1.215V
PWR_VDDQ_PH
PR5110 2D2R5J-1-GP DY
PWR_VDDQ_SNB
PC5118 SC150D50V2KX-2GP

Enable
PG5122 GAP-CLOSE-PWR-3-GP PWR_2D5V_PG PWR_VDDQ_EN
PR5114 1MR2J-1-GP DY
PR5112 0R2J-L-GP DY PM_SLP_S3#
PR5113 0R0402-PAD SM_PGCNTL_R PWR_VTT_EN

APL5934 for 2D5V

5V_S5 PC5167 SC1U25V2KX-1-DLGP
3D3V_S5 PR5166 10K2R2F-2-GP
PR5167 0R0402-PAD
PC5166 SCD1U25V2KX-1-DL-GP SC 1115
PWR_2D5V_PG PM_SLP_S4# PWR_2D5V_EN
PU5166 APL5934KAI-TRG-GP-U 074.05934.003D
2nd = 074.94611.003D
VCNTL POK EN VIN#9 VIN#5 VOUT#4 VOUT#3 FB GND PWR_2D5V_FB
PC5168 SC10U6D3V3MX-DL-GP
Design current=700mA
2D5V_S3
R1 PR5170 20K4R2F-GP DY
R2 PR5171 13K7R2F-GP
PC5169 SC68P50V2JN-1DLGP
PC5170 SC22U6D3V3MX-2DL-GP
PC5171 SC10U6D3V3MX-DL-GP
Vo=0.8x(1+R1/R2)
=0.8x(1+29.4/13.7)
=2.516V

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Power_(5388_VDDQ/VTT)
Size: A2 | Document Number: Jedi15"/17" WHL-U | Rev: A00
Date: Wednesday, January 09, 2019 | Sheet 51 of 106

Main Func = PWR.Plane.Regulator_1D0V

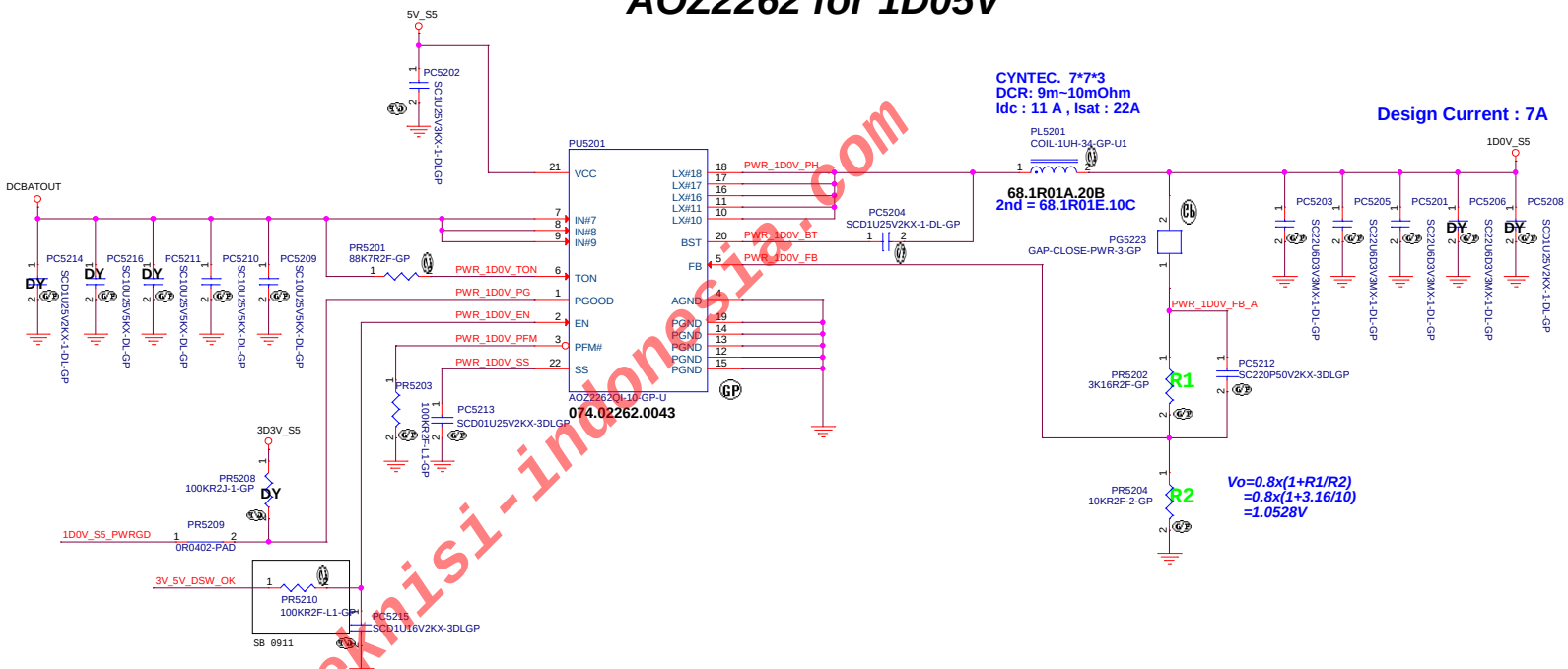
OFFPAGE-Signal

OFFPAGE-GAP

1D0V_S5_PWRGD

3V_5V_DSW_OK

AOZ2262 for 1D05V



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: (Reserved)

Size	Document Number	Rev
Custom	Jedi15"/17" WHL-U	A00

Date: Tuesday, January 08, 2019 Sheet 52 of 106

Main Func = 1D8V

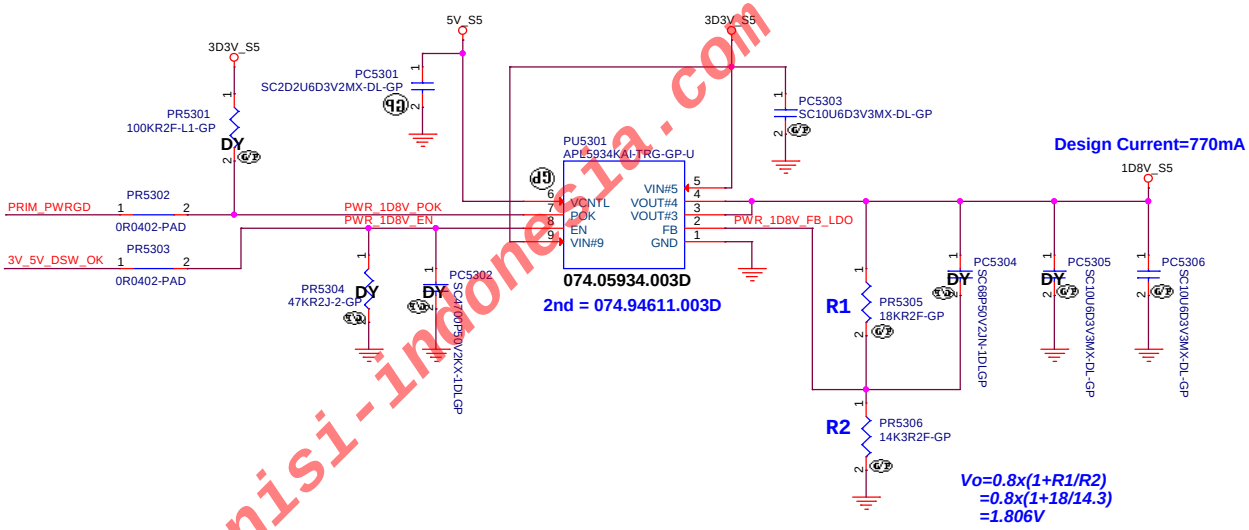
OFFPAGE-Signal

24,40 PRIM_PWRGD

25,52 3V_5V_DSW_OK

OFFPAGE-GAP

APL5934 for 1D8V_S5



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)*

Size	Document Number	Rev
A3	*Jedi15"/17" WHL-U*	*A00*

Date: Tuesday, January 08, 2019 Sheet 53 of 106

Main Func = 2D5V/ 1D8V

<Core Design>

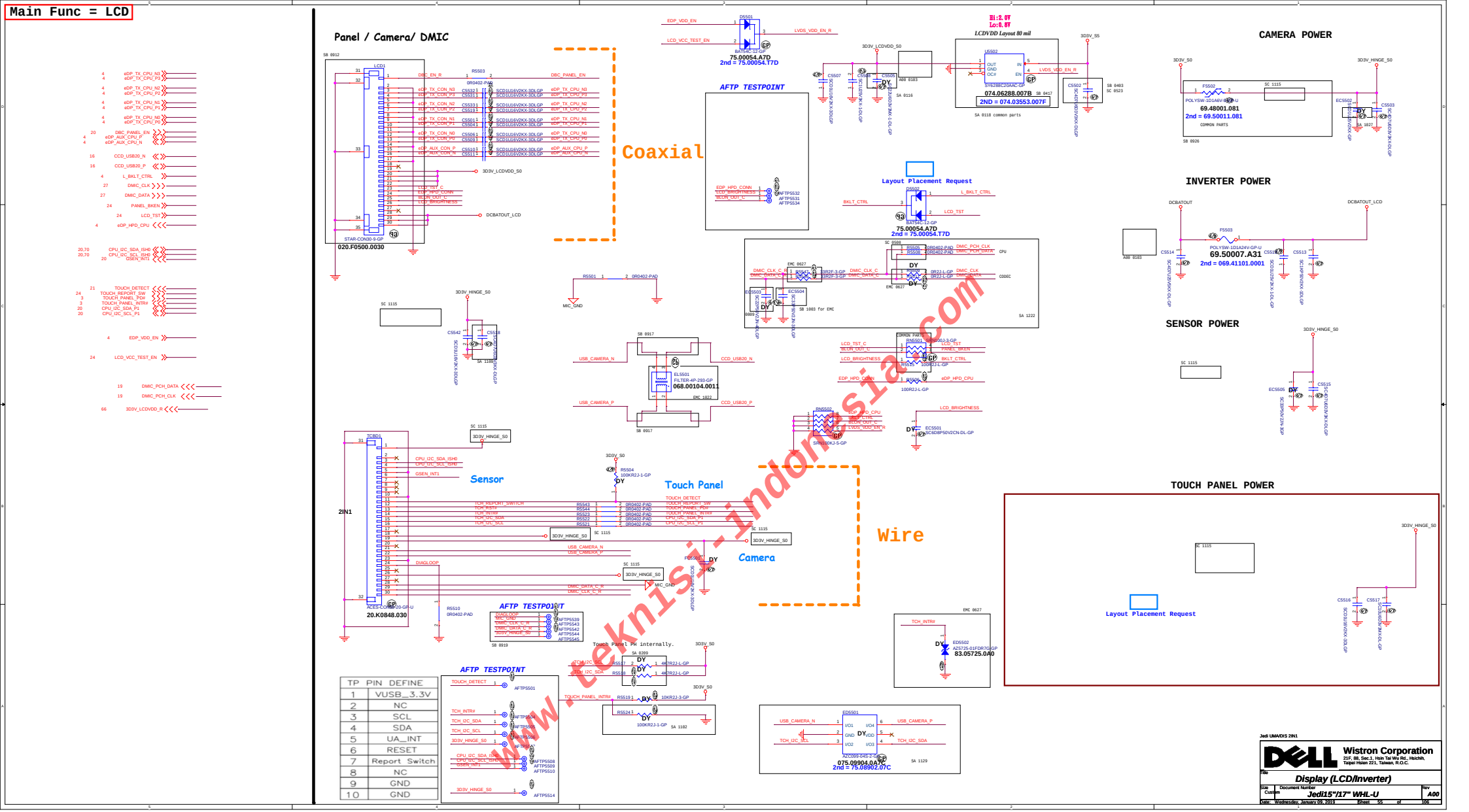
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: (Reserved)

Size: A3 | Document Number: Jedi15"/17" WHL-U | Rev: A00

Date: Tuesday, January 08, 2019 | Sheet 54 of 106

Main Func = LCD



Jedi UMA/DIS 2IN1

Wistron Corporation
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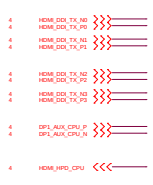
Taipei Hsien 221, Taiwan, R.O.C.

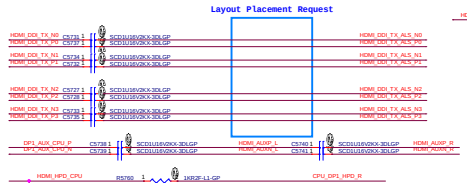
Title: Display (CRT/IR Camera)

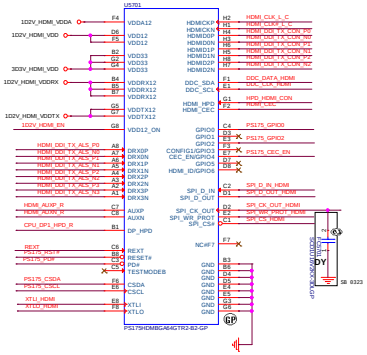
Size	Document Number	Rev
A2	Jedi15"/17" WHL-U	A00

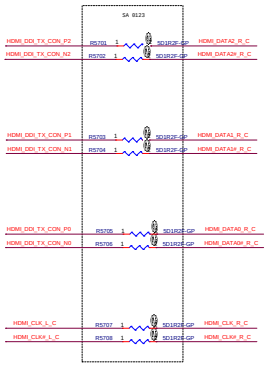
Date: Tuesday, January 08, 2019 Sheet 56 of 106

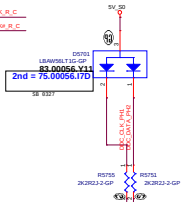
Main Func = HDMI

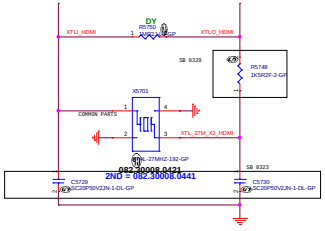


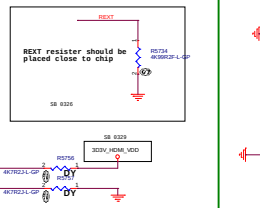


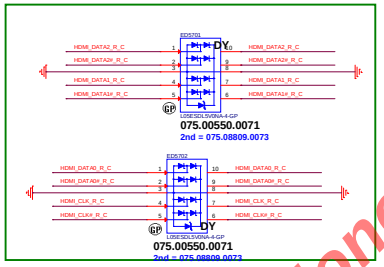


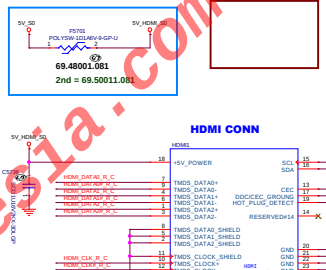


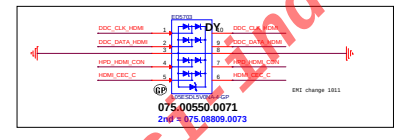


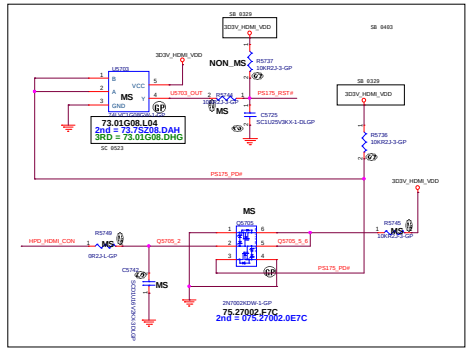




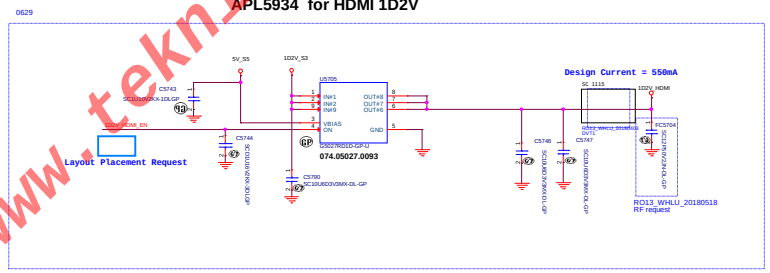


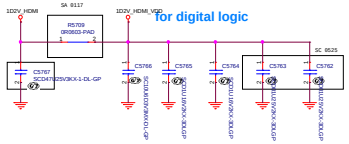


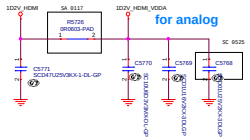


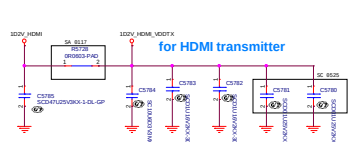


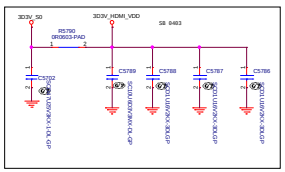
HDMI POWER

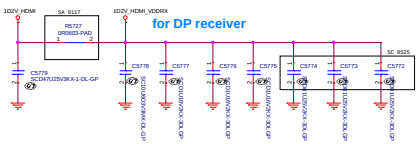












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Jedi UMA/DIS 2IN1

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Display (RSVD) DP

Size	Document Number	Rev
Custom	Jedi15"/17" WHL-U	A00

Date: Tuesday, January 08, 2019 Sheet 58 of 106

(Blanking)

Jedi UMA/DIS 2IN1

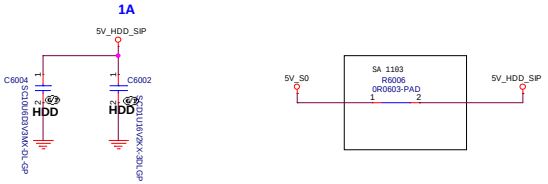
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

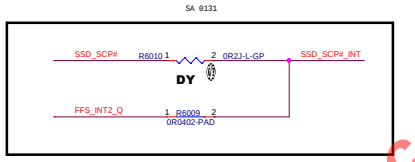
Title: Display (RSVD) DVI

Size: A3 | Document Number: Jedi15"/17" WHL-U | Rev: A00

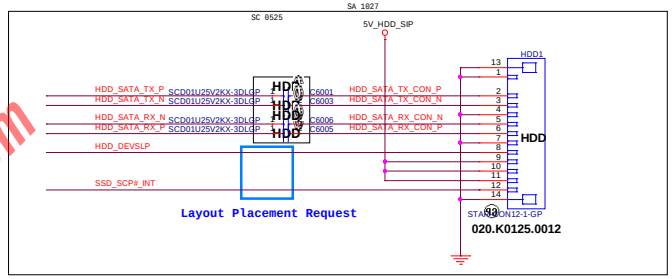
Date: Tuesday, January 08, 2019 | Sheet 59 of 106

Main Func = HDD

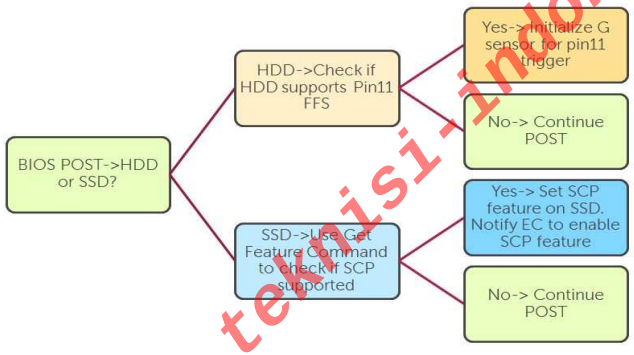


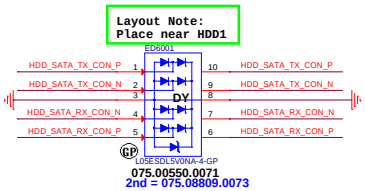


SATA HDD Connector



- BIOS today already check whether the device is HDD and whether it supports FFS before enabling sensor chip to trigger pin11. The plan is to add a check on the SSD path to decide if device supports SCP and notify EC whether to support SCP.





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Title: *INT IO (HDD/ODD)*

Size: A2 | Document Number: Jedi15"/17" WHL-U | Rev: A00

Date: Tuesday, January 08, 2019 | Sheet 60 of 106

Main Func = WLAN

3.3 Peak current consumption

Table 3-4 Peak current consumption

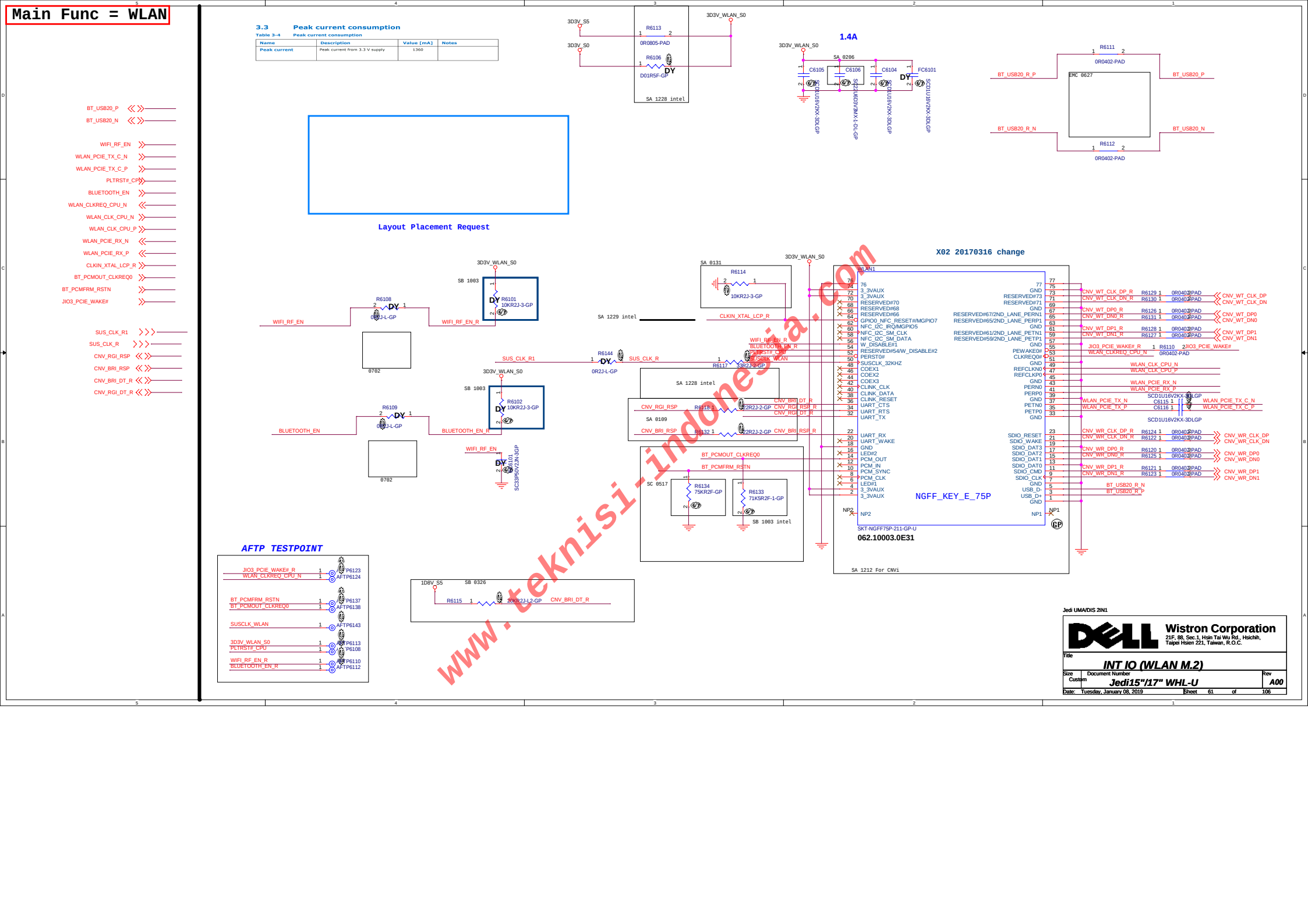
Name	Description	Value [mA]	Notes
Peak current	Peak current from 3.3 V supply	1360	

Layout Placement Request

1.4A

X02 20170316 change

AFTP TESTPOINT



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Title: INT IO (WLAN M.2)

Size: Custom | Document Number: Jedi15"/17" WHL-U | Rev: A00

Date: Tuesday, January 08, 2019 | Sheet 61 of 106

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Jedi UMA/DIS 2IN1

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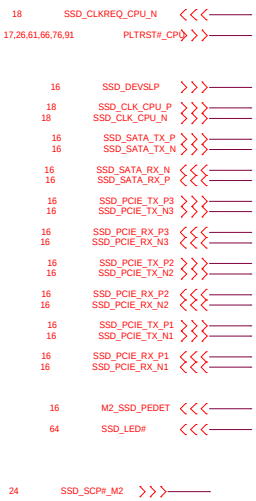
Title

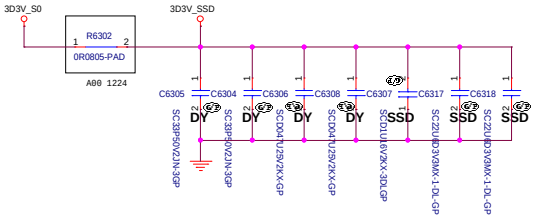
INT IO (RSVD) WWAN

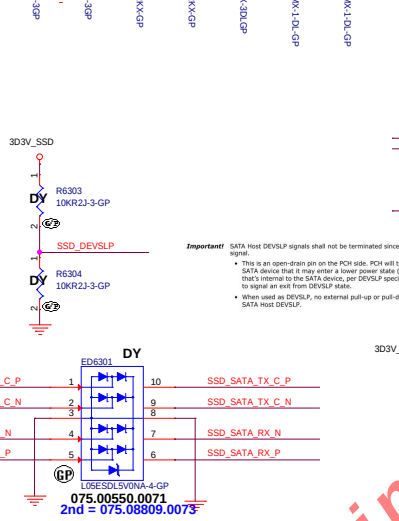
Size	Document Number	Rev
A4	Jedi15"/17" WHL-U	A00

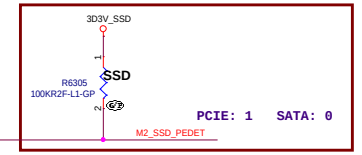
Date: Tuesday, January 08, 2019 Sheet 62 of 106

Main Func = SSD M.2









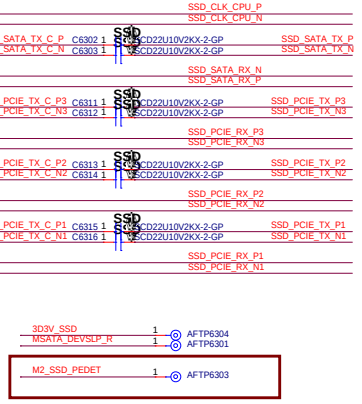


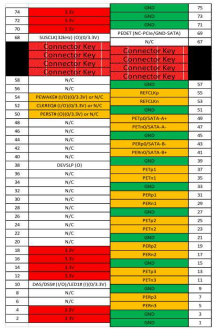
Table 13-12. SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[2]	None	None[3]

Notes:

1. Design Constraint: For PCIe only application, please refer to the PCIe guidelines for details.
2. Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the Rx 10 nF capacitor can be removed if DC coupled ODDs / devices are NOT used.
3. Design Constraint: For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
4. Design Constraint: For PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
5. Design Constraints, Required: Refer to the Chapter 3, "General Differential Signals Design Guidelines"" along with the additional guidelines in this section for all design optimization guidelines.
6. Design Constraint: For PCIe* lane that needs to support either **PCIe* Gen2 devices** or **PCIe* Gen3 devices**, follow the PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**

Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform



Jedi UMA/DIS 2IN1

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Title: INT IO (SSD M.2/ eMMC)

Size: Custom | Document Number: Jedi15"/17" WHL-U | Rev: A00

Date: Wednesday, January 09, 2019 | Sheet 63 of 106

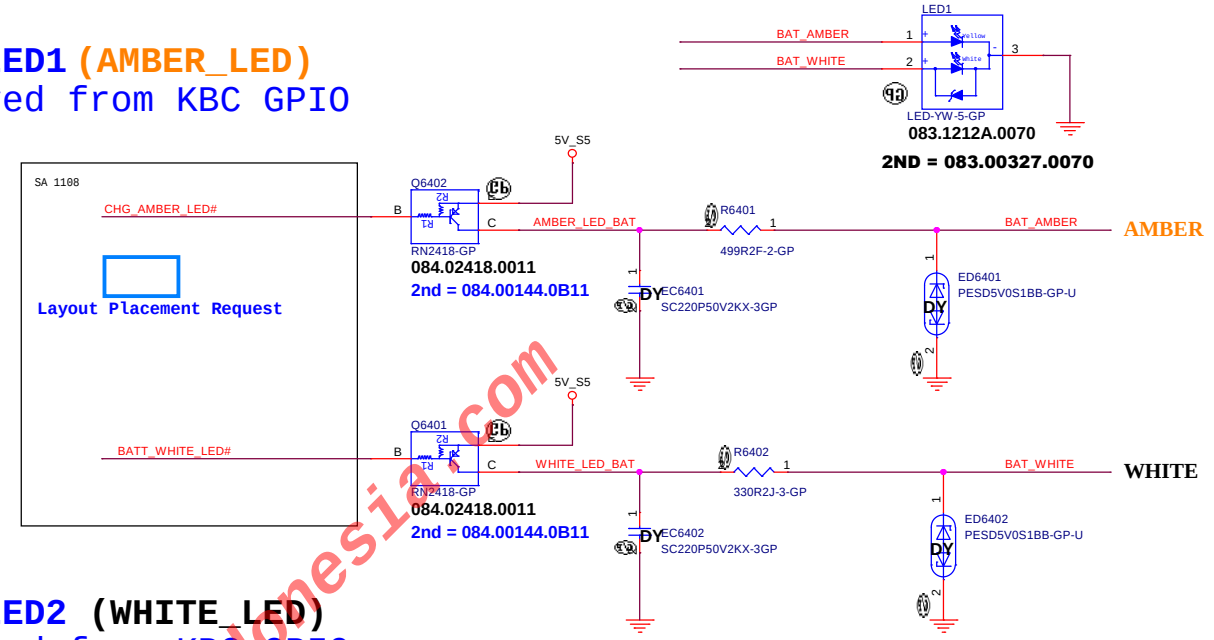
Main Func = Power BTN

24,90 CHG_AMBER_LED#

24 BATT_WHITE_LED#

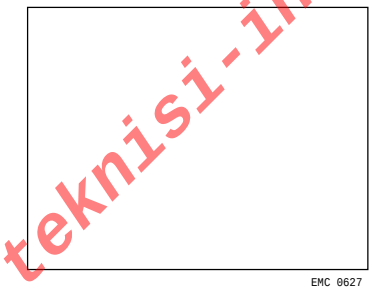
Battery LED1 (AMBER_LED)

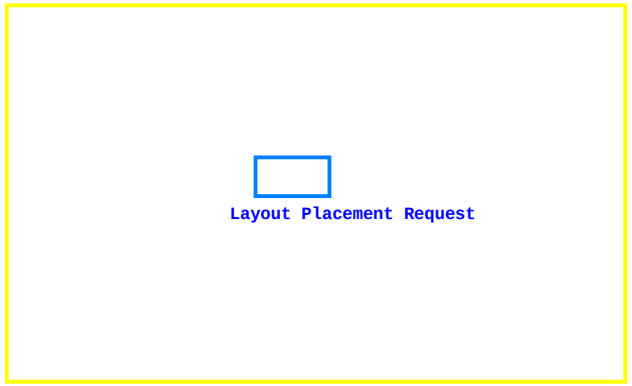
Low actived from KBC GPIO



Battery LED2 (WHITE_LED)

Low actived from KBC GPIO

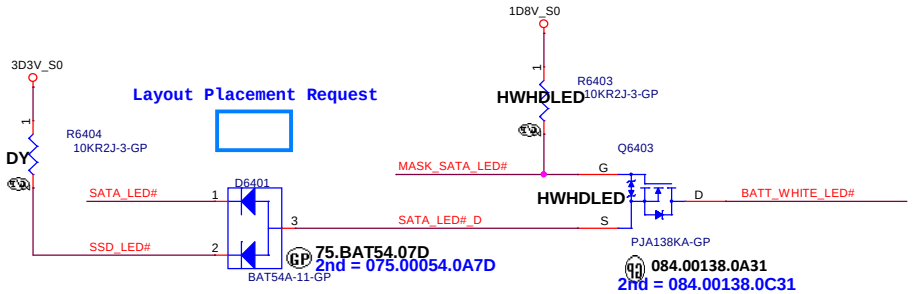




16 SATA_LED#

63 SSD_LED#

24 MASK_SATA_LED#



Jedi UMA/DIS 2IN1

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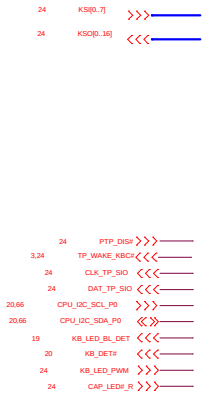
Title: LED / Button / Power Button

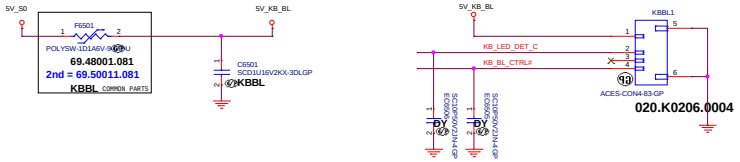
Size: A3 | Document Number: Jedi15"/17" WHL-U | Rev: A00

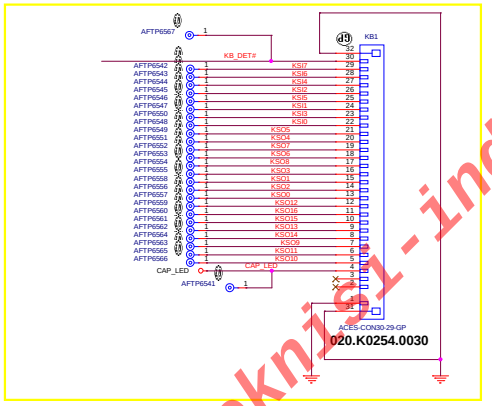
Date: Tuesday, January 08, 2019 | Sheet 64 of 106

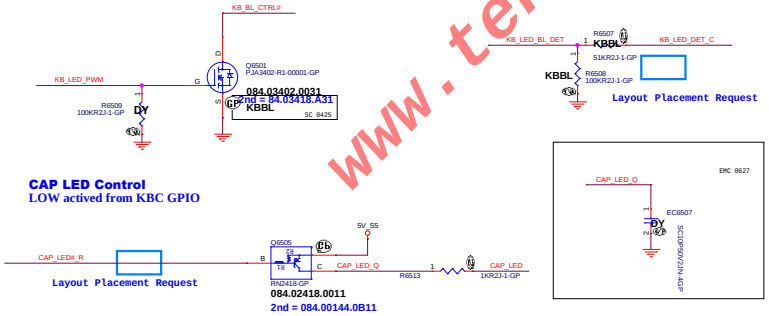
Main Func = Keyboard

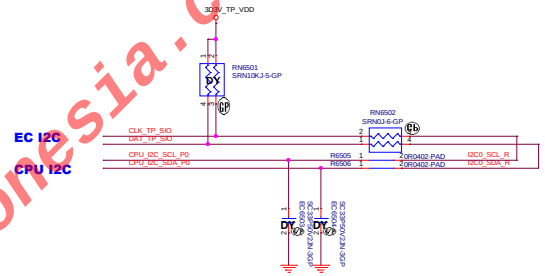
Main Func = TPAD

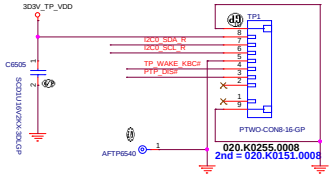


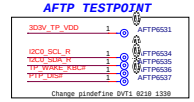




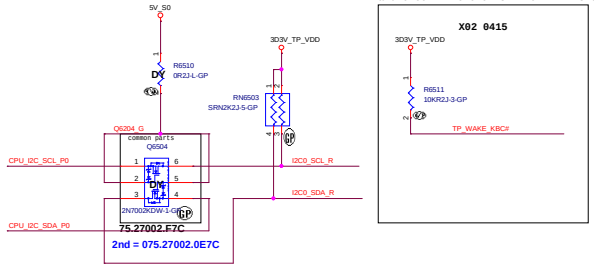








Need to check if it is Active High or Active Low and check if there is PH on TPAD side.



Pin number	Pin name
1	VDD
2	DAT(I2C)
3	CLK(I2C)
4	GND
5	ATTN
6	GPIO
7	DAT(PS2)
8	CLK(PS2)

Jedi UMA/DIS 2IN1

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Title: INT IO (KB/TP)

Size	Document Number	Rev
Custom	Jedi15"/17" WHL-U	A00
Date: Tuesday, January 08, 2019	Sheet 65 of 105	

Main Func = IO Connector

20,24,69 LID_CL_SIO#
24,90 KBC_PWRBTN#
17,26,61,63,76,91 PLTRST#_CPU
16 USB2_USB20_P
16 USB2_USB20_N
16 USB1_USB20_P
16 USB1_USB20_N
16 USB1_USB30_RX_N
16 USB1_USB30_RX_P
16 USB1_USB30_TX_N
16 USB1_USB30_TX_P
16 USB2_USB30_RX_N
16 USB2_USB30_RX_P
16 USB2_USB30_TX_N
16 USB2_USB30_TX_P
17,40,51 PM_SLP_S4#
20,24,69 LID_CL_SIO_TAB#
24 NC_U3_PD#_EC SC 1121
24 FPR_SCAN#
24 USB_EN#
16 USB_OC1#
16 FP1_USB20_N
16 FP1_USB20_P
27,66 AUD_SENSE
27,29,66 RING2_R
27,29,66 RING2_R
27,29,66 RING2_R
27,29,66 RING2_R
27,29,66 SLEEVE_R
27,29,66 SLEEVE_R
27,29,66 SLEEVE_R
27,29,66 SLEEVE_R
29,66 AUD_HP1_JACK_R1
29,66 AUD_HP1_JACK_L1
20,65 CPU_I2C_SDA_P0
20,65 CPU_I2C_SCL_P0
44 PWR_CHG_CSOP_R
44 PWR_CHG_CSON_R
55 3D3V_LCDVDD_R

IOBD1
STAR-CON50-3-GP
020.F1405.0050
USB1_USB20_P
USB1_USB20_N
USB2_USB20_P
USB2_USB20_N
USB2_USB30_RX_P
USB2_USB30_RX_N
USB2_USB30_TX_P
USB2_USB30_TX_N
USB1_USB30_RX_P
USB1_USB30_RX_N
USB1_USB30_TX_P
USB1_USB30_TX_N
FP1_USB20_P
FP1_USB20_N
5V_S5
NC_U3_PD#_EC
LID_CL_SIO#
3D3V_S5
RTC_VCC
PM_SLP_S4#
FPR_SCAN#
KBC_PWRBTN#
USB_EN#
USB_OC1#
AUD_AGND
AUD_HP1_JACK_L1
AUD_SENSE 27,66
SLEEVE_R 27,29,66
SLEEVE_R 27,29,66
SLEEVE_R 27,29,66
RING2_R 27,29,66
RING2_R 27,29,66
RING2_R 27,29,66
AUD_HP1_JACK_R1 29,66
AUD_AGND

AFTP TESTPOINT

USB1_USB20_P AFTP6603
USB1_USB20_N AFTP6604
USB2_USB20_P AFTP6605
USB2_USB20_N AFTP6606
FP1_USB20_P AFTP6609
FP1_USB20_N AFTP6610
FPR_SCAN# AFTP6619
USB_EN# AFTP6620
USB_OC1# AFTP6621
LID_CL_SIO# AFTP6622
LID_CL_SIO_TAB# AFTP6623
KBC_PWRBTN# AFTP6624
PM_SLP_S4# AFTP6625
5V_S5 AFTP6626
5V_S5 AFTP6627
5V_S5 AFTP6628
5V_S5 AFTP6629
5V_S5 AFTP6630
3D3V_S5 AFTP6633
3D3V_S5 AFTP6634
AUD_AGND AFTP6635
SLEEVE_R AFTP6636
RING2_R AFTP6637
AUD_SENSE AFTP6638
AUD_HP1_JACK_L1 AFTP6639
AUD_HP1_JACK_R1 AFTP6640
SB 0919

3D3V_S5
R6615 100KR2J-1-GP
LID_CL_SIO_TAB#

EMI Reserve , 20141118

KBC_PWRBTN# PLTRST#_CPU
ED6602 ED6603
SC381P50V2JN-3GP

Layout Placement Request

AFTP TESTPOINT

KBC_PWRBTN# AFTP6601
KBC_PWRBTN# AFTP6602

FP1_USB20_P ED6608 AZ5725-01FDR7G-GP
FP1_USB20_N ED6607 AZ5725-01FDR7G-GP
USB2_USB20_P ED6605 AZ5725-01FDR7G-GP
USB2_USB20_N ED6606 AZ5725-01FDR7G-GP
USB1_USB20_P ED6609 AZ5725-01FDR7G-GP
USB1_USB20_N ED6610 AZ5725-01FDR7G-GP
DY
EMC 0627

SA 1025
ED6602
USB2_USB30_RX_P
USB2_USB30_RX_N
USB2_USB30_TX_P
USB2_USB30_TX_N
L05ESDL5V0NA-4-GP
075.00550.0071
2nd = 075.08809.0073
ED6604
USB1_USB30_RX_P
USB1_USB30_RX_N
USB1_USB30_TX_P
USB1_USB30_TX_N
L05ESDL5V0NA-4-GP
075.00550.0071
2nd = 075.08809.0073

EMC 0627

<Core Design>

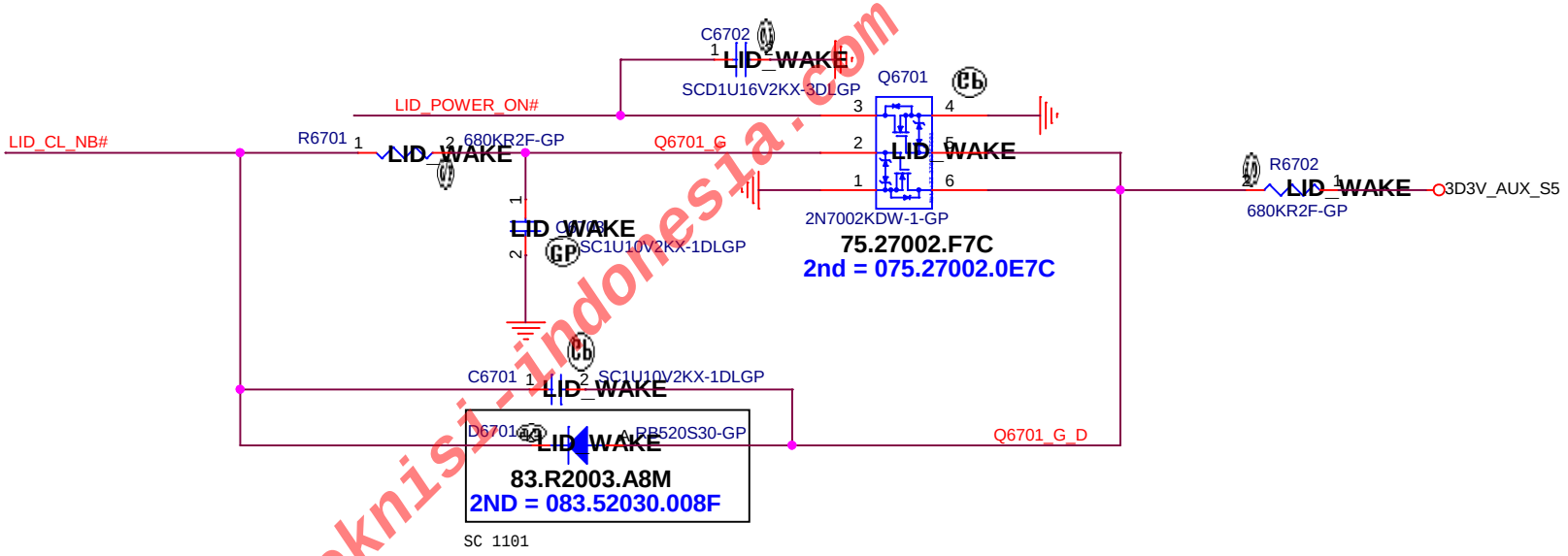
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board Connector
Size: A2
Document Number: Jedi15"/17" WHL-U
Rev: A00
Date: Tuesday, January 08, 2019
Sheet 66 of 106

Main Func = HALL SENSOR

69 LID_CL_NB#

4 LID_POWER_ON#



<Core Design>

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Title: Lid_Wake

Size	Document Number	Rev
A4	Jedi15"/17" WHL-U	A00

Date: Tuesday, January 08, 2019 Sheet 67 of 106

Main Func = Debug

24 HOST_DEBUG_TX

20 UART_2_CTXD_DRXD

20 UART_2_CRXD_DTXD

18,24 ESPI_CLK

18,24 ESPI_RESET#

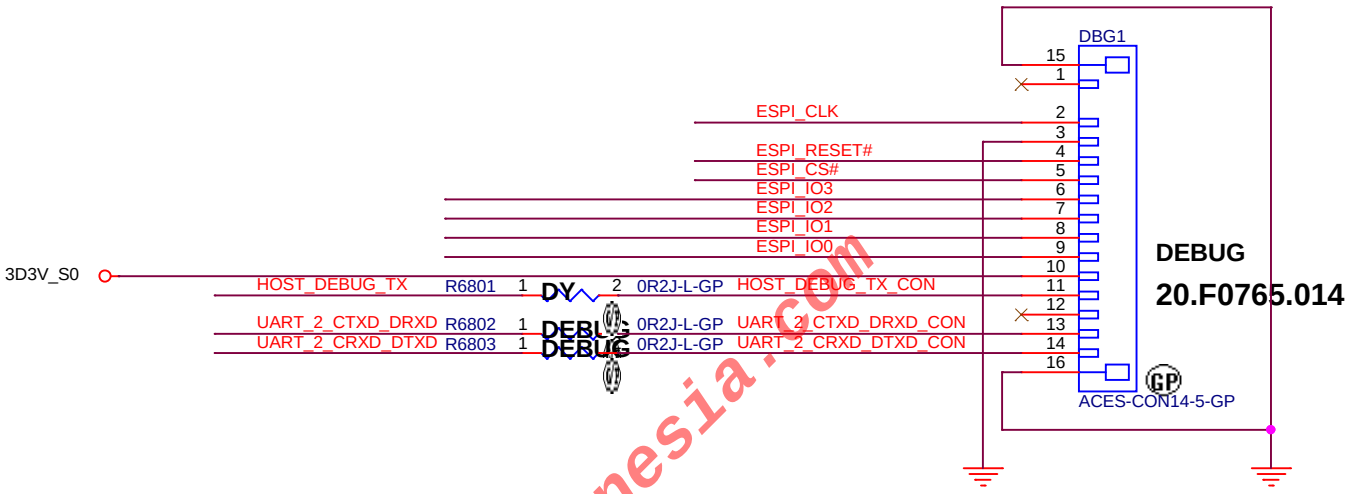
18,24 ESPI_CS#

18,24 ESPI_IO[3..0]

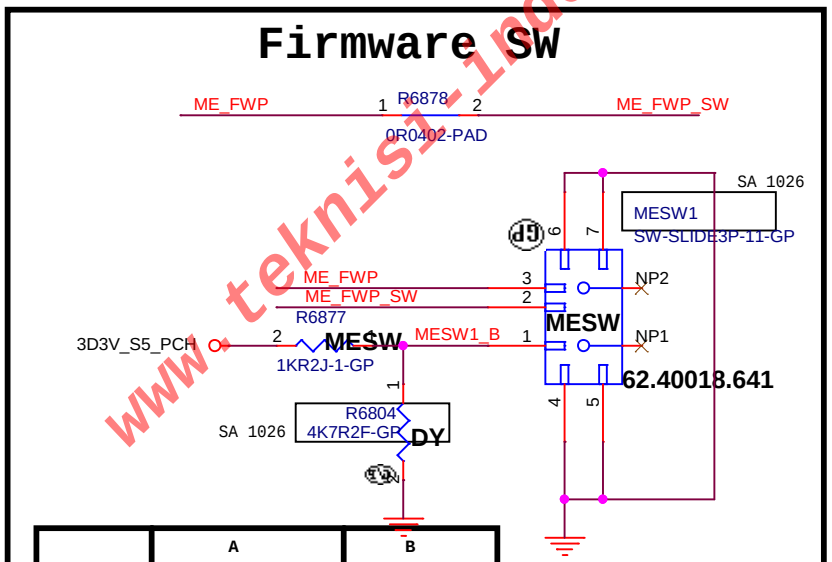
24 ME_FWP

19 ME_FWP_SW

Debug Connector



Firmware SW



	A	B
ME_FWP	Low	High
	Normal Operation (Default)	Override

Jedi UMA/DIS 2IN1

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Debug (LPC debug)

Size	Document Number	Rev
A4	Jedi15"/17" WHL-U	A00

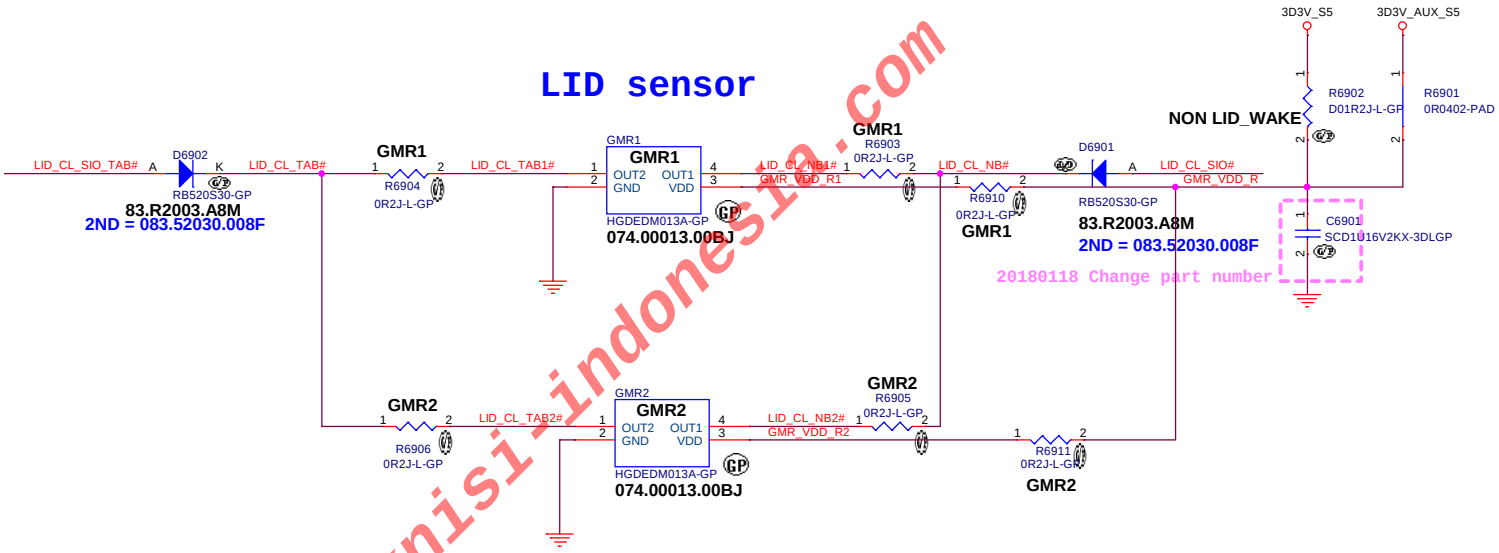
Date: Tuesday, January 08, 2019 Sheet 68 of 106

20,24,66 LID_CL_SIO#

0,24,66 LID_CL_SIO_TAB#

67 LID_CL_NB#

LID sensor



Jedi UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Sensor (RSVD)

Size	Document Number	Rev
A3	Jedi15"/17" WHL-U	A00

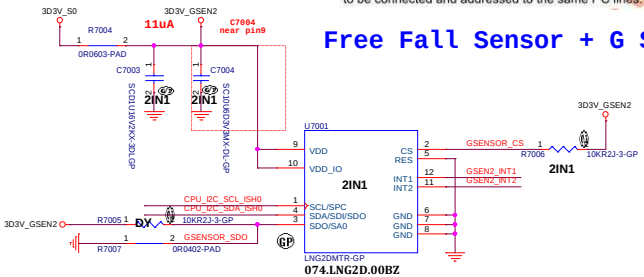
Date: Tuesday, January 08, 2019 Sheet 69 of 106

Main Func = Free Fall Sensor

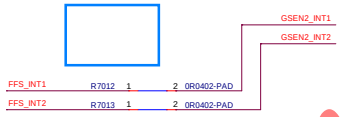
20,55 CPU_I2C_SCL_ISH0
20,55 CPU_I2C_SDA_ISH0
20 GSEN2_INT1
18 FFS_INT1
20 FFS_INT2
60 FFS_INT2_Q

The slave address (SAD) associated to the LNG2DM is 010100xb. The **SDO/SA0** pad can be used to modify the least significant bit of the device address. If the SA0 pad is connected to a voltage supply, LSB is '1' (address 0101001b) or, if the SA0 pad is connected to ground, the LSB value is '0' (address 0101000b). This solution permits two different accelerometers to be connected and addressed to the same I²C lines.

Free Fall Sensor + G Sensor



Layout Placement Request



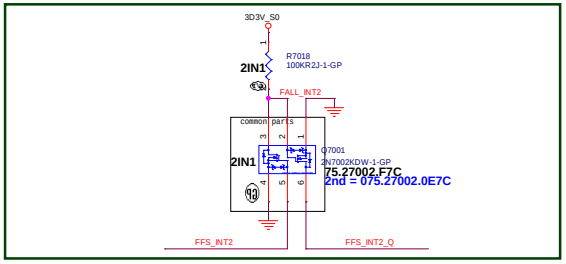
Layout Placement Request

combine G

Layout Placement Request

Note:
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

Please help to close with U7001



Note:
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

Jedi UMA/DIS 2IN1

Wistron Corporation
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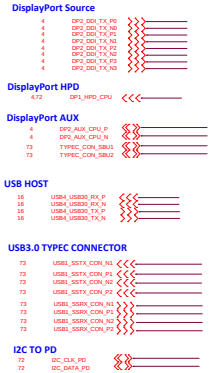
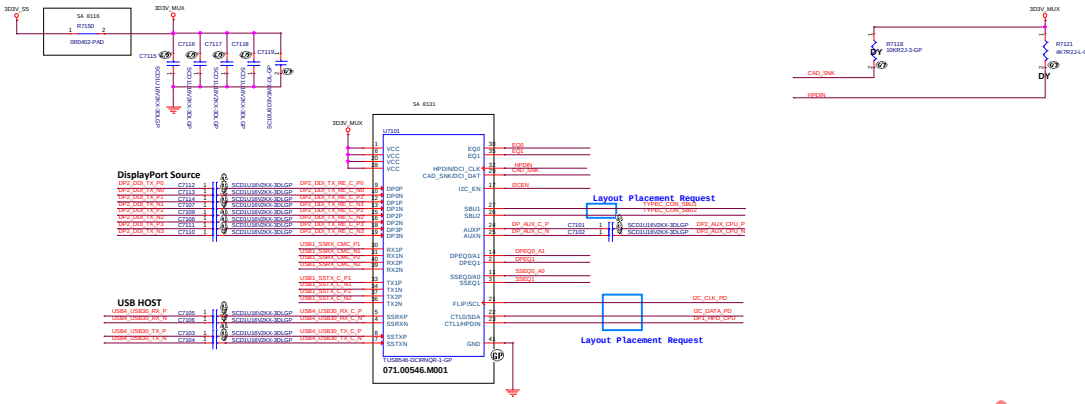
Title: Sensor (G-sensor)
Size: A2 | Document Number: Jedi15"/17" WHL-U | Rev: A00
Date: Tuesday, January 08, 2019 | Sheet 70 of 106

Main Func = TYPEC MUX





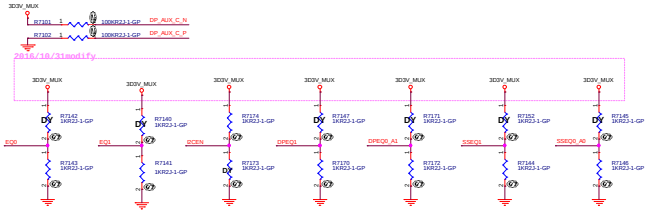
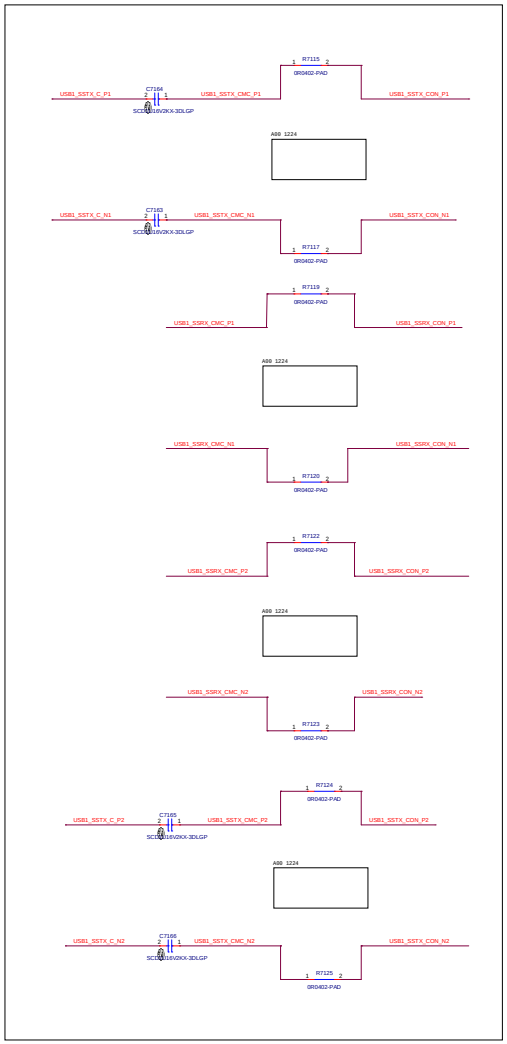


Table 1. 4-Level Control Pin Settings

LEVEL	SETTINGS
0	Option 1: Tie 1 KΩ 5% to GND. Option 2: Tie directly to GND.
R	Tie 20 KΩ 5% to GND.
F	Float (leave pin open)
1	Option 1: Tie 1 KΩ 5%to V_{CC}. Option 2: Tie directly to V_{CC}.



Jedi USA/DES 2IN1

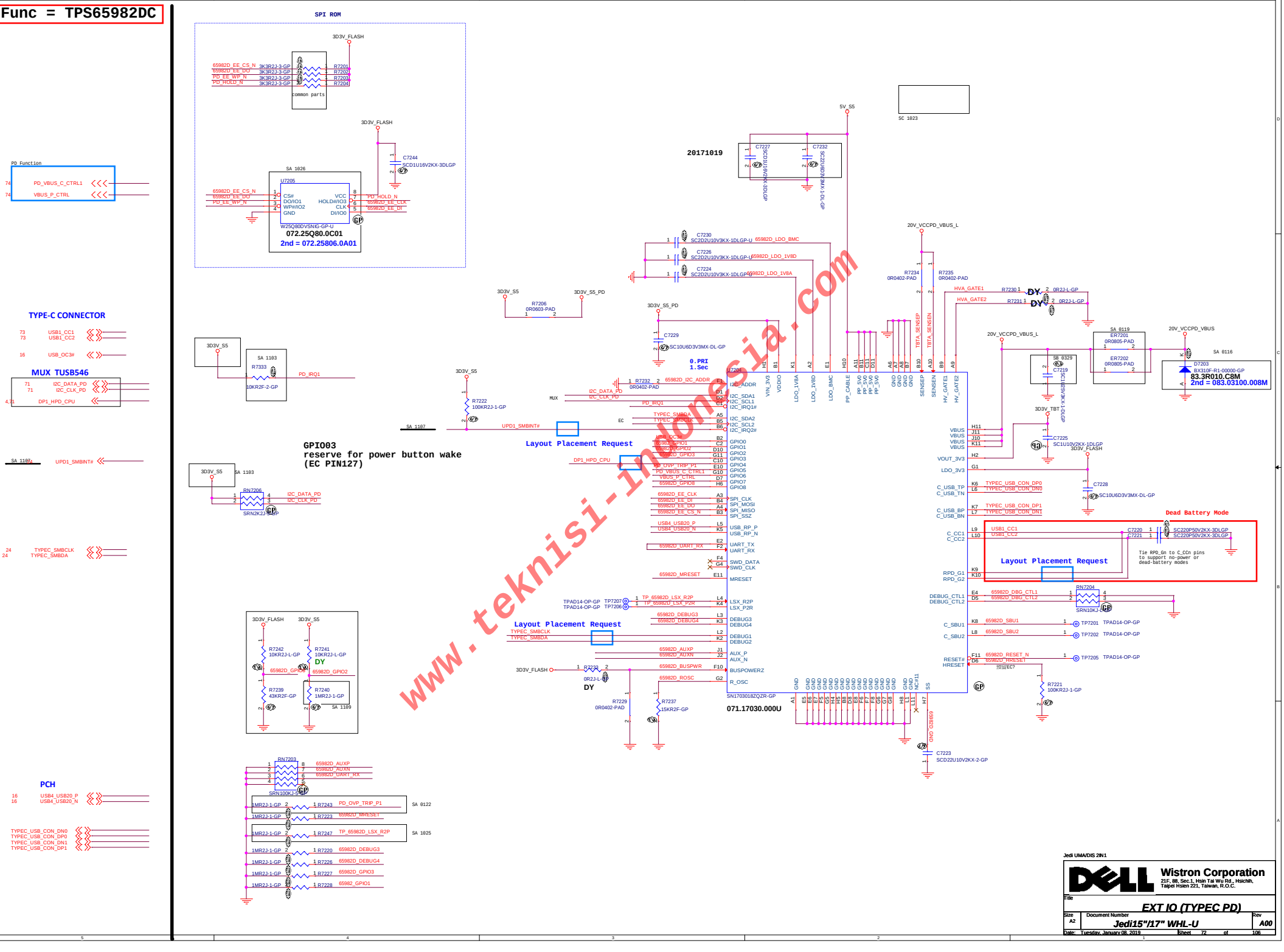
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: EXT IO(TBT(1/3)/Re-timer)

Size	Document Number	Rev
A1	Jedi15"/17" WHL-U	A00

Date: Tuesday, January 08, 2019 Sheet 71 of 106

Main Func = TPS65982DC



Main Func = TYPEC CONNECTOR

SB Layout Placement Request

RO13_20170821 for EMI request

ED7303 — L05ESDL5V0NA-4-GP
075.00550.0071
2nd = 075.08809.0073

ED7304 — AZC099-04S-2-GP
075.09904.0A7C
2nd = 75.08902.07C

ED7301 — L05ESDL5V0NA-4-GP
075.00550.0071
2nd = 075.08809.0073

ED7302 — L05ESDL5V0NA-4-GP
075.00550.0071
2nd = 075.08809.0073

71 USB1_SSRX_CON_N1
71 USB1_SSRX_CON_P1
71 USB1_SSRX_CON_N2
71 USB1_SSRX_CON_P2
71 USB1_SSTX_CON_N1
71 USB1_SSTX_CON_P1
71 USB1_SSTX_CON_N2
71 USB1_SSTX_CON_P2
72 TYPEC_USB_CON_DN0
72 TYPEC_USB_CON_DP0
72 TYPEC_USB_CON_DN1
72 TYPEC_USB_CON_DP1
71 TYPEC_CON_SBU1
71 TYPEC_CON_SBU2

check
72 USB1_CC1
72 USB1_CC2

SC 1121 — SA 1226

AFTP TESTPOINT
AFTP7317
AFTP7318

20V_VCCPD_VBUS

SB 0329

Layout Placement Request

TYPEC1 — SKT-USB30-64-GP
062.10009.M029

SB Layout Placement Request
EMC 1022 — EL7301 FILTER-4P-293-GP
068.00104.0011

SB Layout Placement Request
SB Layout Placement Request
EMC 1022 — 068.00104.0011 FILTER-4P-293-GP EL7312

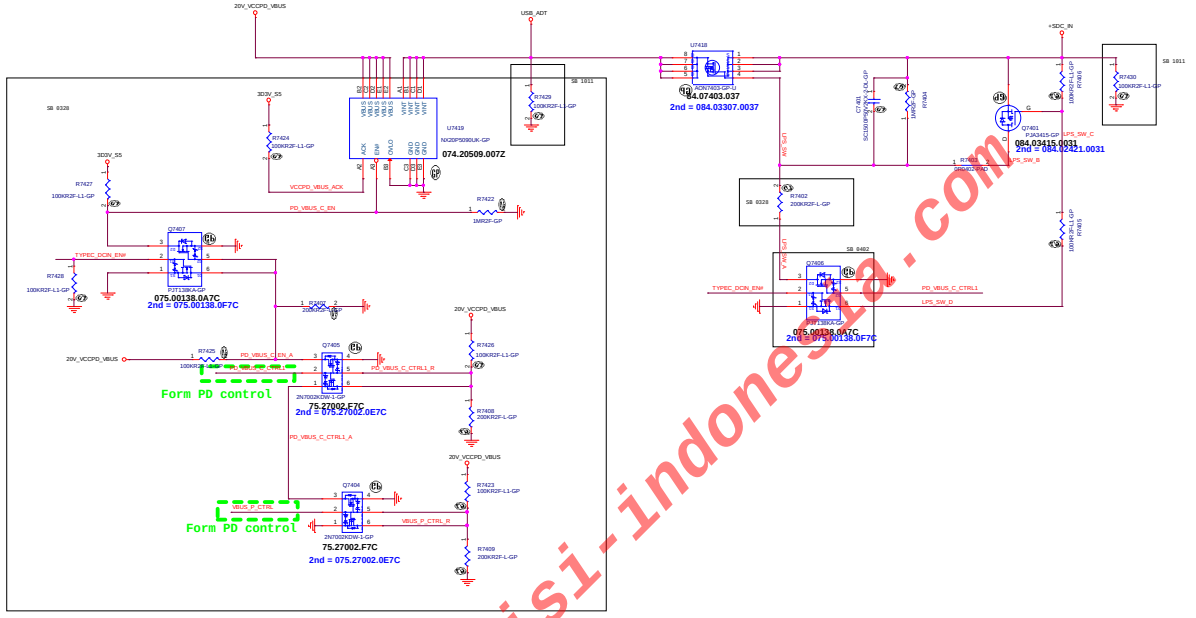
SB Layout Placement Request

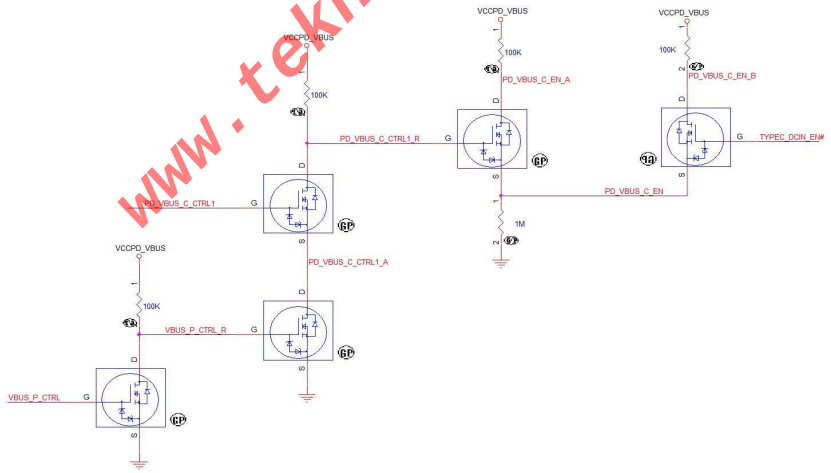
Jedi UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: EXT IO_(TBT(3/3)/TypeC CON)
Size: A3 | Document Number: Jedi15"/17" WHL-U | Rev: A00
Date: Tuesday, January 08, 2019 | Sheet 73 of 106

Main Func = TYPEC protect





Jedi UMA/DIS 2IN1

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: EXT IO (LPS)

Size	Document Number	Rev
A1	Jedi15"/17" WHL-U	A00

Date: Tuesday, January 08, 2019 Sheet 74 of 106

<Core Design>

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Title

EXT IO (TYPEC Redriver/MUX)

Size	Document Number	Rev
A	Jedi15"/17" WHL-U	A00

Date: Tuesday, January 08, 2019 Sheet 75 of 106

Main Func = dGPU

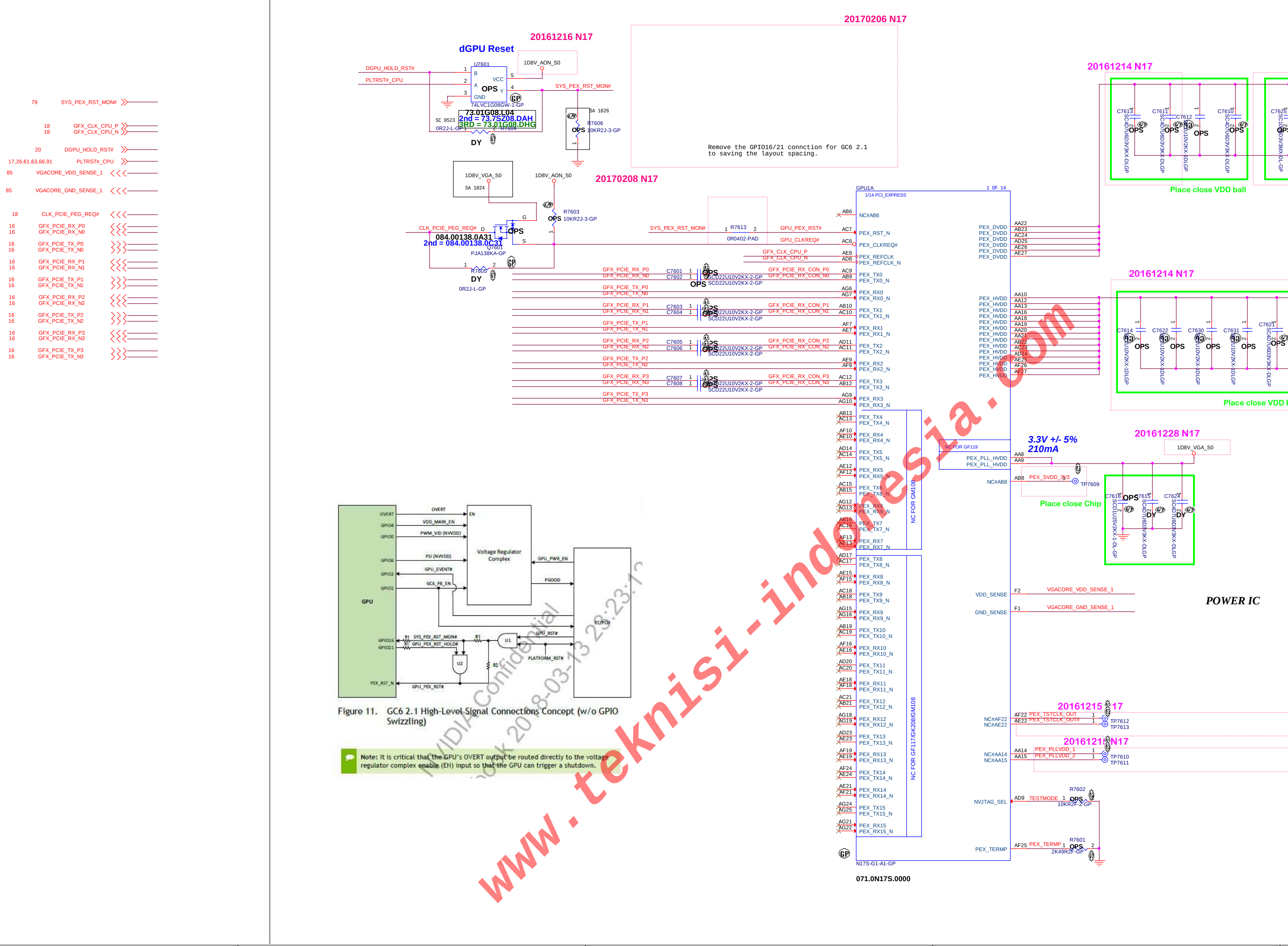


Figure 11. GC6 2.1 High-Level Signal Connections Concept (w/o GPIO Swizzling)

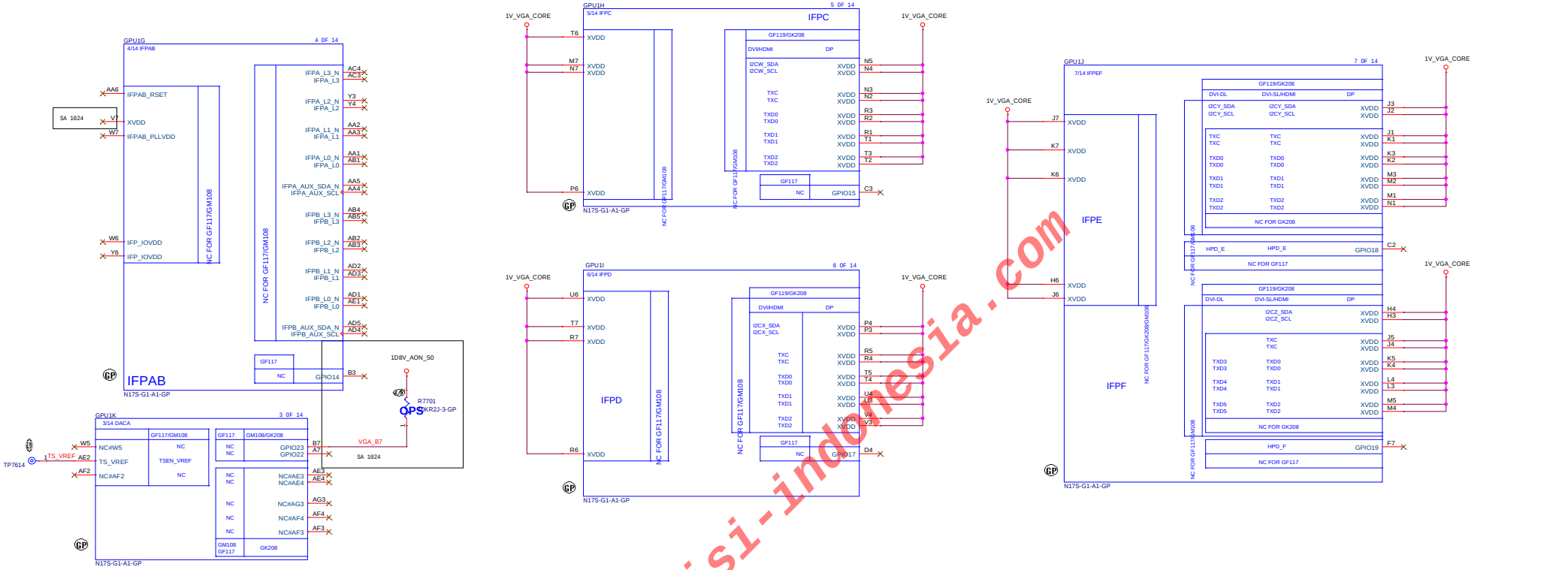
Note: It is critical that the GPU's OVERT output be routed directly to the voltage regulator complex enable (EN) input so that the GPU can trigger a shutdown.

Table 6. PEX Core and IO Supply Decoupling and Filtering

GPU	Capacitor Type		Footprint	Population N16	Population N17	Location
N16 PEX_IOVDD (N17 PEX_DVDD) Supply Rail						
GB2B-64, GB2C-64	1.0 µF	X6S	0402	1	1	Under GPU
	4.7 µF	X6S	0603	0	1	Under GPU
	4.7 µF	X6S	0603	1	2	Near GPU
	10 µF	X6S	0805	0	2	Midway between GPU and Power Supply
	22 µF	X6S	0805	0	1	Midway between GPU and Power Supply
N16 PEX_IOVDDQ (N17 PEX_HVDD) Supply Rail						
GB2B-64, GB2C-64	1.0 µF	X6S	0402	1	4	Under GPU
	4.7 µF	X6S	0603	1	2	Near GPU
	10 µF	X6S	0805LP	1	2	Midway between GPU and Power Supply
	22 µF	X6S	0805LP	1	1	Midway between GPU and Power Supply

GPU	Capacitor Type		Footprint	Population N16	Population N17	Location
PEX_PLL_HVDD Supply Rail						
GB2B-64, GB2C-64	0.1 µF	X7R	0402	1	1	Near GPU

Main Func = dGPU



Jedi UMA/DIS 2IN1

Wistron Corporation
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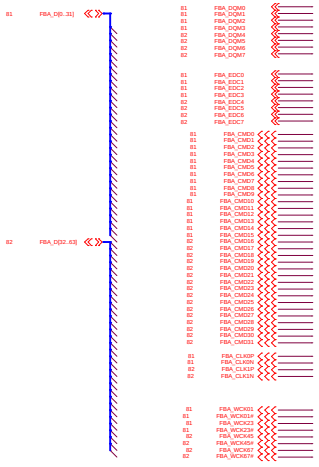
Taipei Hsien 221, Taiwan, R.O.C.

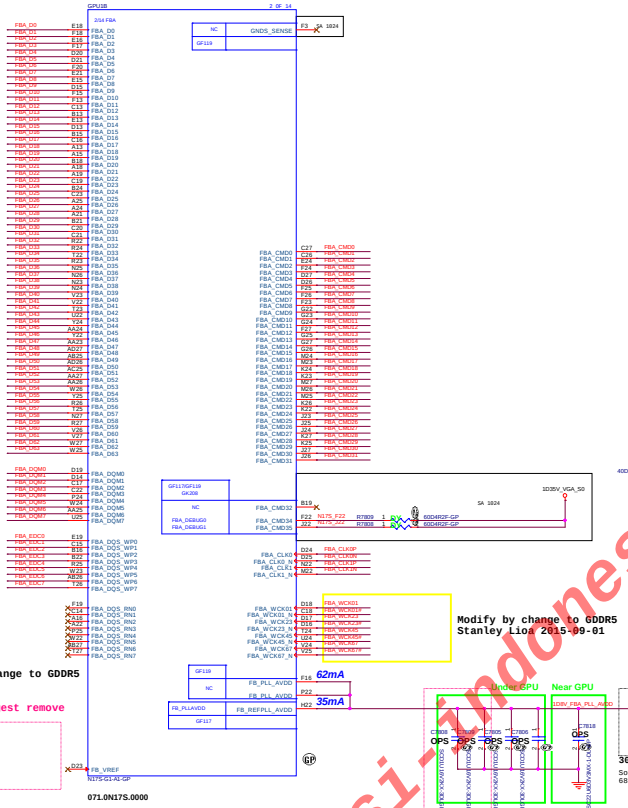
Title: GPU (DIGITAL 2/5)

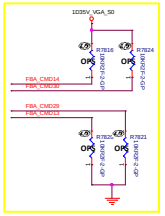
Size: A2 | Document Number: Jedi15"/17" WHL-U | Rev: A00

Date: Tuesday, January 08, 2019 | Sheet 77 of 106

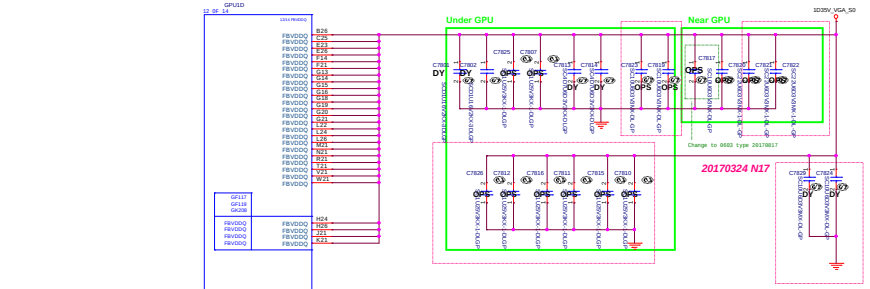
Main Func = dGPU







Note:
Reference NV-DDR5 CRB and DOH70 by GDDR5



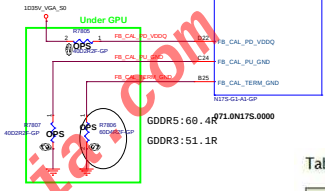


Table 4. Frame Buffer Core and IO Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population N16	Population N17	Location
FBVDD/Q Supply Rail for GDDR5					
GB2B-64, GB2C-64	0.1 µF	X7R	0402	2	0	Under GPU
	1 µF	X7R	0603	2	8	Under GPU
	4.7 µF	X6S	0603	2	0	Under GPU
	10 µF	X6S	0603	0	2	Under GPU
	10 µF	X6S	0603	1	1	Near GPU
	22 µF	X6S	0603W	1	3	Near GPU

Table 5. Frame Buffer PLLs Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population N16	Population N17	Location
FB PLL Supply Rail for GDDR5					
GB2B-64, GB2C-64	0.1 µF	X7R	0402	2	4	Under GPU
	22 µF	X6S	0805	1	1	Near GPU
	Bead Type				
	30 Ω (ESR=0.010 Ω)	0603	1	1	Near GPU

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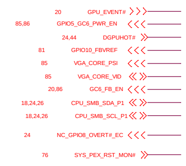
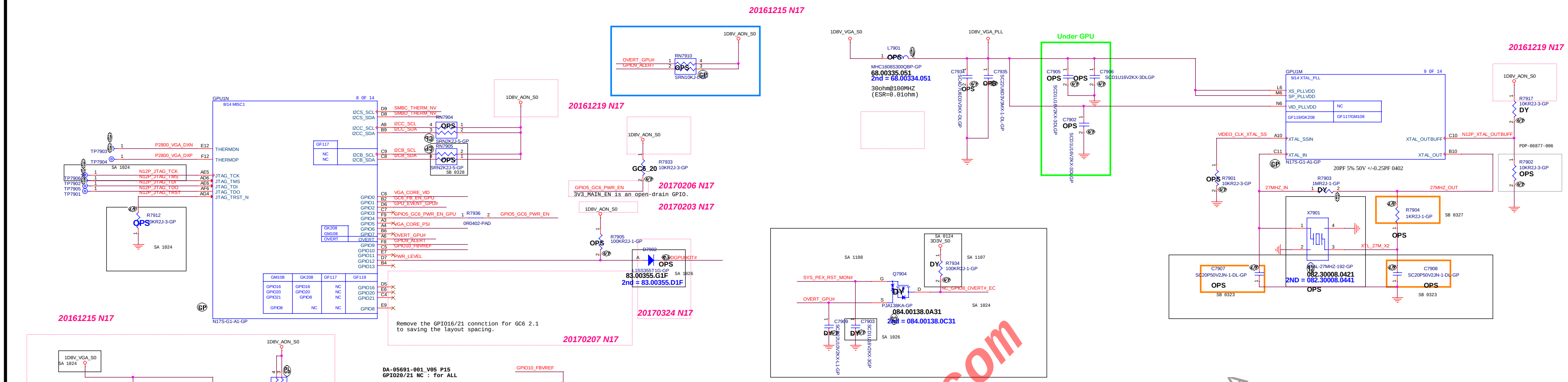
GPU (VRAM 3/5)

Jedi15"/17" WHL-U

A00

Main Func = dGPU





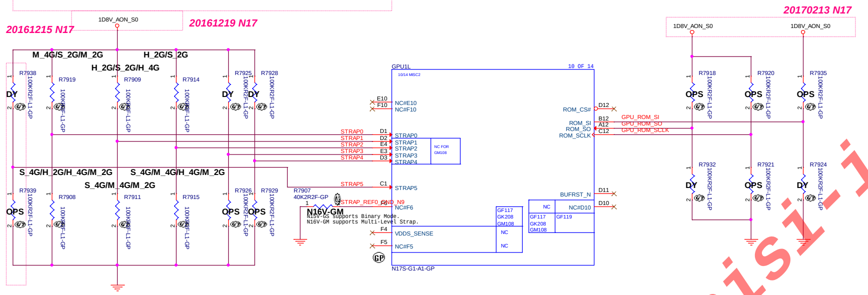


Table 5.5 SORx_EXPOSED Strap Enablement for Down Designs

Row Index	Strap Pins see Note			Resulting SORx_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_ EXPOSED	SOR2_ EXPOSED	SOR1_ EXPOSED	SOR0_ EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
8	H	H	H	ENABLED	disabled	disabled	disabled
0	H	H	M	disabled	disabled	disabled	disabled
	M	X	X	(Reserved; do not configure)			
	All other Strap Configurations			(Reserved)			

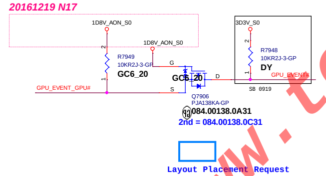
Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000) Samsung 2G
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004) Micron 2G
H	L	H	5 (0x0005) Hynix 2G
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

20161215 N17

Table 5.6 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

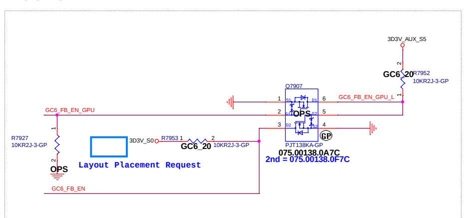
Strap Pins Note 1			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0

20161219 N17



Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32 512Mx16	1.35V	Samsung	K4G80325FB-HC28	B-die	0x0	7 Gbps	N/A	Full	Production ready
			Samsung	K4G80325FB-HC25	B-die	0x0	8 Gbps	N/A	N/A	Substitution allowed with waiver[2]
			Micron	MT51J256M32HF-70:A	A-die	0x1	7 Gbps	N/A	Full	Production ready
			Micron	MT51J256M32HF-80:A	A-die	0x1	8 Gbps	N/A	N/A	Substitution allowed with waiver[2]
			Hynix	H5GC8H24MJR-R0C	M-die	0x2	7 Gbps	N/A	Full	Post production ready
			Hynix	H5GQ8H24MJR-R4C	M-die	0x2	8 Gbps	N/A	N/A	Substitution allowed with waiver[2]
			Micron	MT51J256M32HF-70:B	B-die	0x4	7 Gbps	N/A	Full	Post production ready
			Micron	MT51J256M32HF-80:B	B-die	0x4	8 Gbps	N/A	N/A	Substitution allowed with waiver[2]
			Hynix	H5GC8H24AJR-R0C	A-die	0x5	7 Gbps	N/A	Full	Post production ready
			Hynix	H5GC8H24AJR-R2C	A-die	0x5	8 Gbps	N/A	N/A	Substitution allowed with waiver[2]
4 Gb	128Mx32 256Mx16	1.35V	Hypix	H5GC4H24AJR-R0C	A-die	0x6	7 Gbps	N/A	Full	Production ready
			Hynix	H5GQ4H24AJR-R4C	A-die	0x6	8 Gbps	N/A	N/A	Substitution allowed with waiver[2]

20161223 N17



Jedi UMA/DIS 2IN1

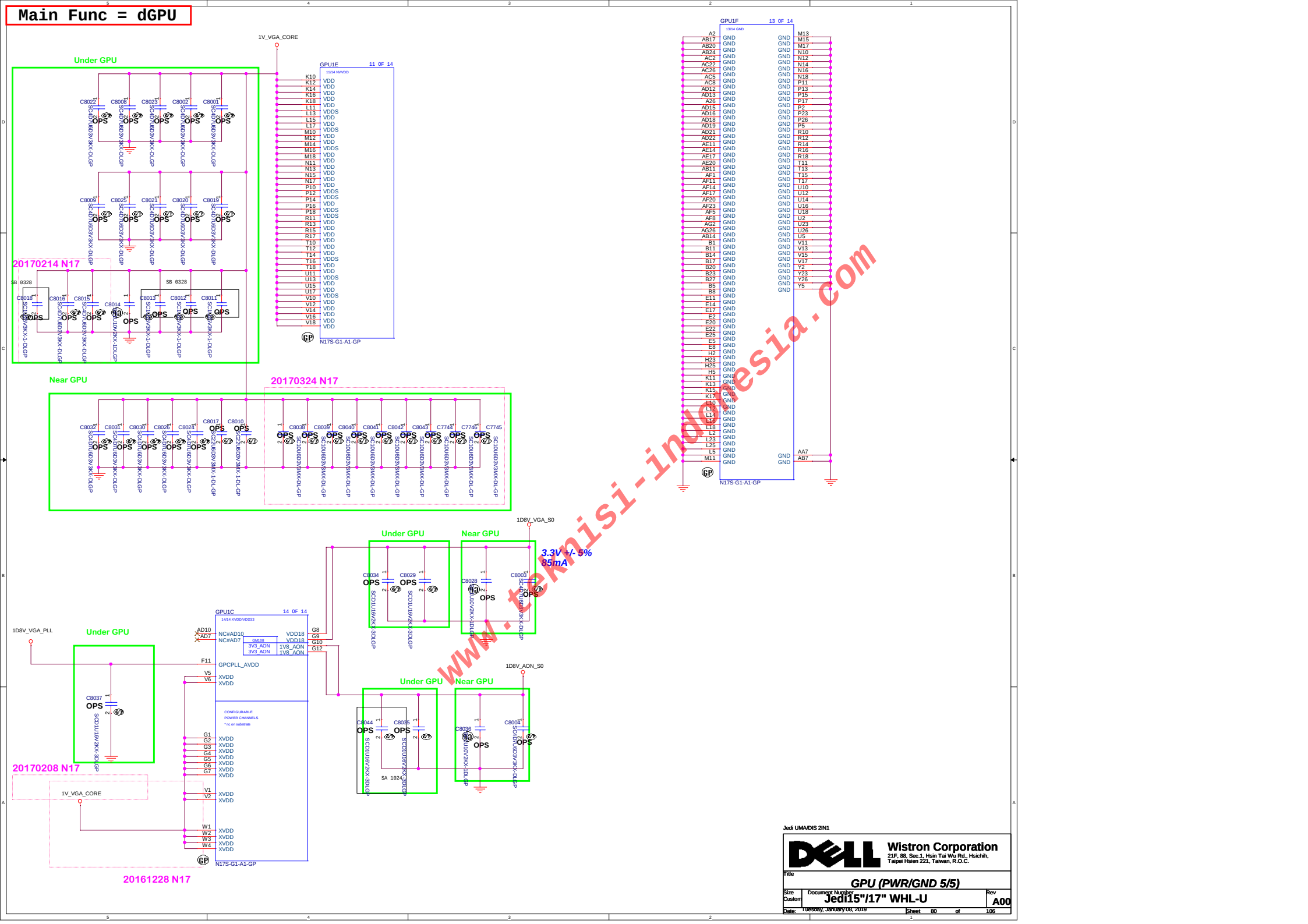
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (GPIO 4/5)

Size: Custom | Document Number: Jedi15"/17" WHL-U | Rev: A00

Date: Tuesday, January 08, 2019 | Sheet 79 of 106

Main Func = dGPU



Jedi UMA/DIS 2IN1

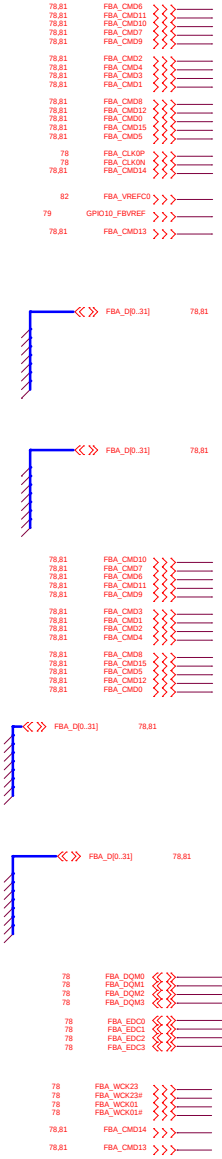
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

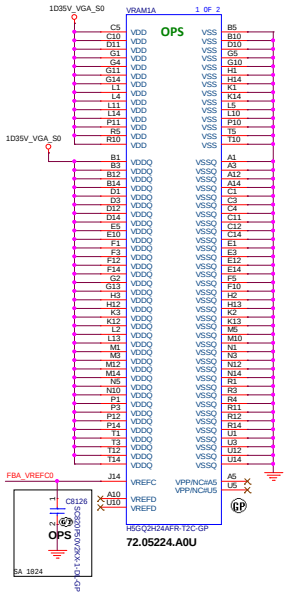
Title: GPU (PWR/GND 5/5)

Size: Custom | Document Number: Jedi15"/17" WHL-U | Rev: A00

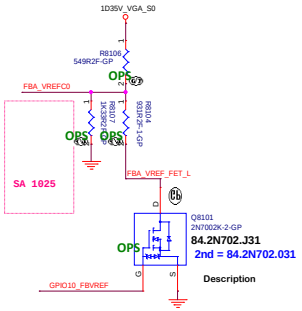
Date: Tuesday, January 08, 2019 | Sheet 80 of 106

SSID = VRAM





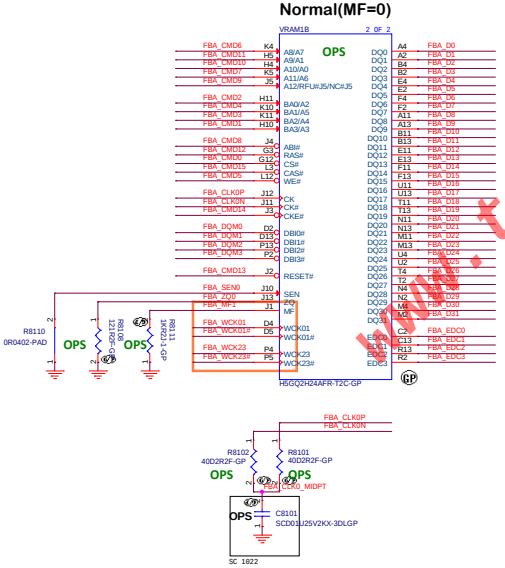
Frame Buffer Patition A-Lower Half



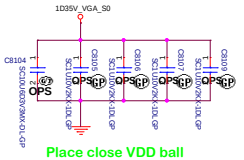
FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low

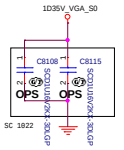
Normal(MF=0)



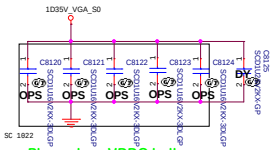
Place close VDD ball



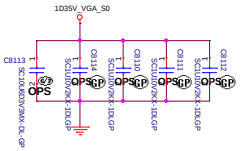
Place close VDD ball



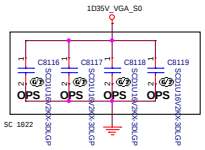
Place close VDD ball



Place close VDDQ ball



Place close VDDQ ball



<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM1.2 (1/4)

Size: Custom | Document Number: Starload-KBL-R GPU | Rev: A00

Date: Tuesday, January 08, 2019 | Sheet 81 of 13

SSID = VRAM

Frame Buffer Patition A-Upper Half

SA 1025

FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low

Mirrored(MF=1)

Place close VDD ball

Place close VDDQ ball

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: GPU-VRAM3.4 (2/4)

Size: Custom | Document Number: Starload-KBL-R GPU | Rev: A00

Date: Tuesday, January 08, 2019 | Sheet 82 of 13

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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *GPU (VRAM5,6 3/4)*

Size	Document Number	Rev
A3	Jedi15"/17" WHL-U	A00

Date: Tuesday, January 08, 2019 Sheet 83 of 106

Jedi UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *GPU (VRAM7,8 4/4)*

Size	Document Number	Rev
A3	Jedi15"/17" WHL-U	A00

Date: Tuesday, January 08, 2019 Sheet 84 of 106

Main Func = dGPU

RT8816B For NVVDD

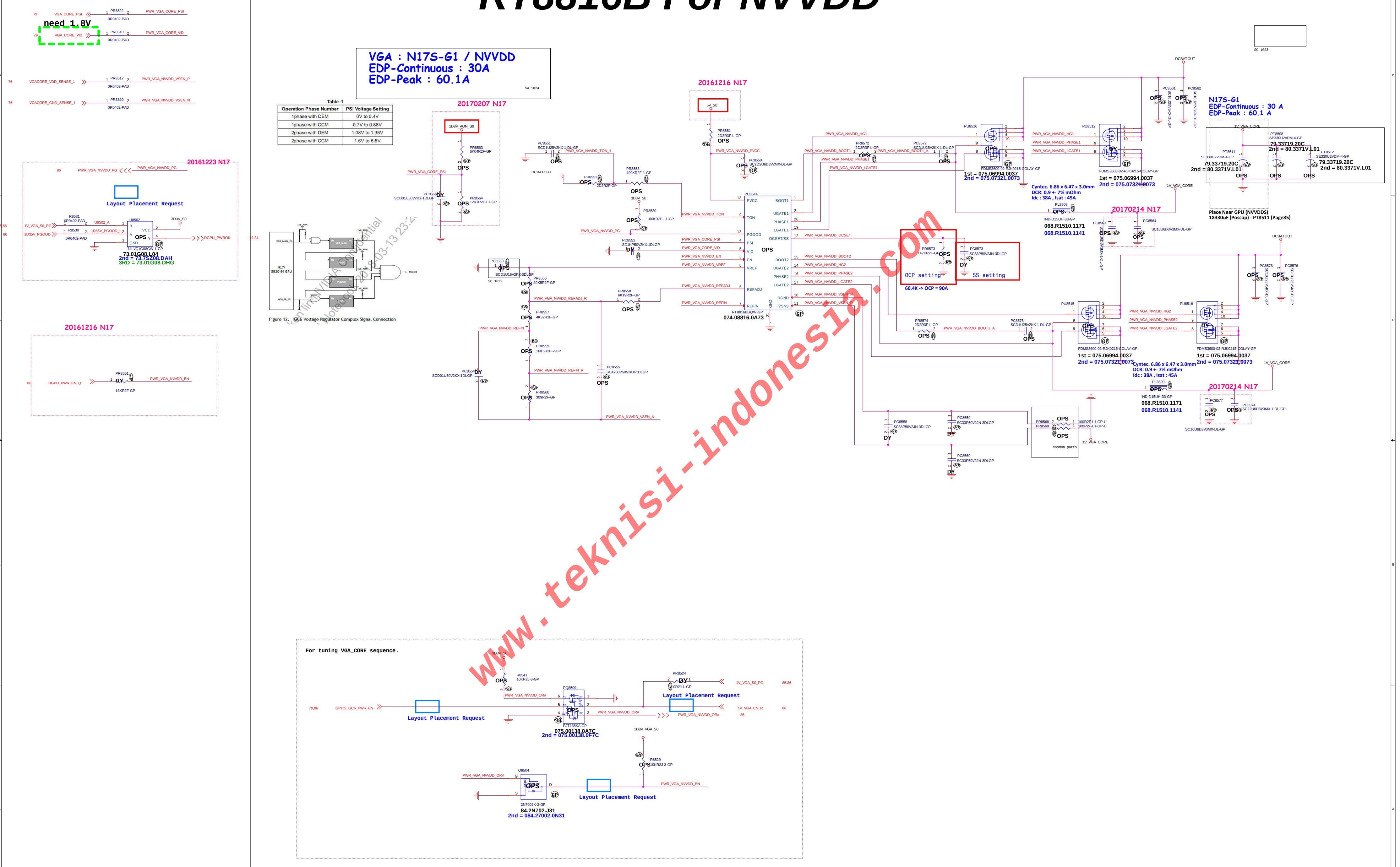


Table 1

Operation Phase Number	PSI Voltage Setting
1phase with DEM	0V to 0.4V
1phase with CCM	0.7V to 0.88V
2phase with DEM	1.08V to 1.35V
2phase with CCM	1.6V to 5.5V

<Core Design>

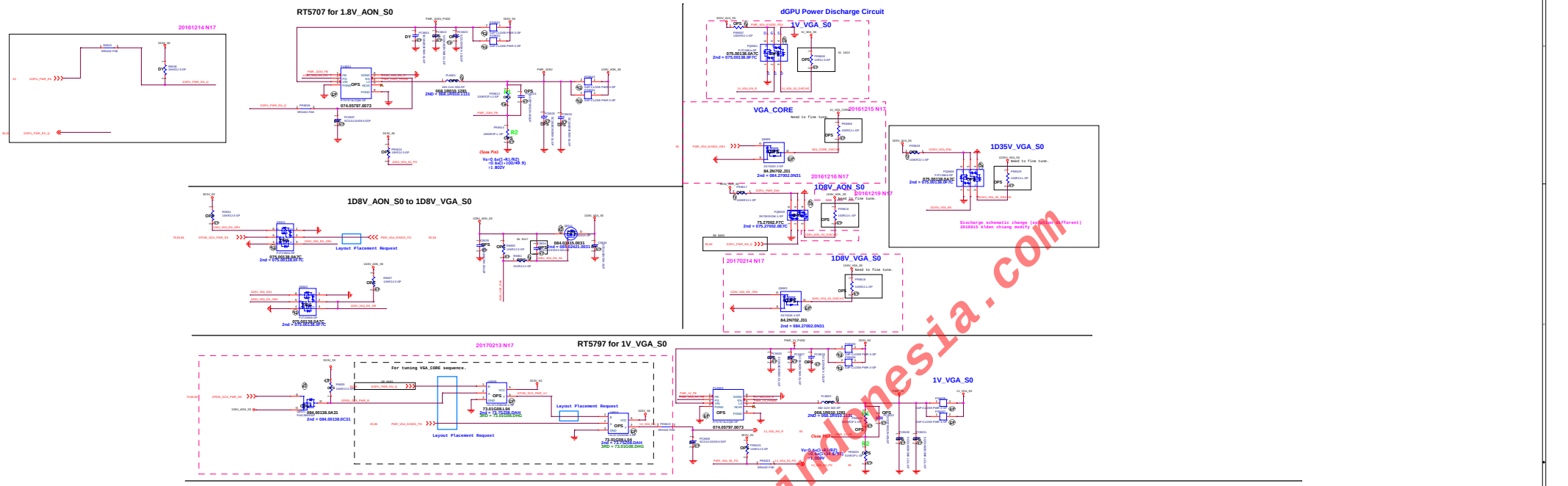
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

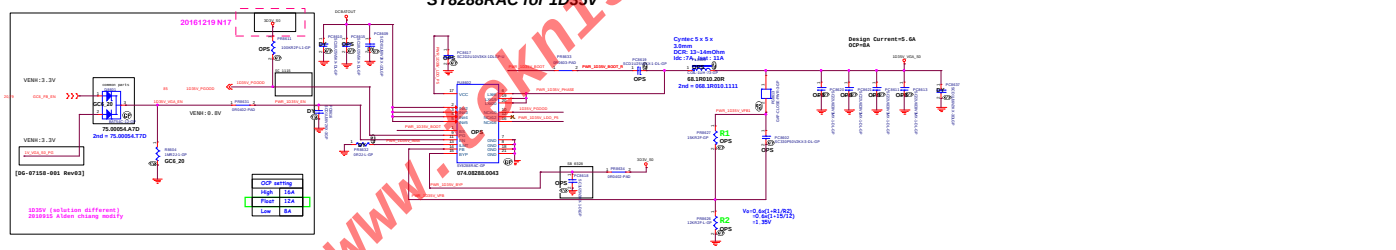
Title: VGA Power B

Size: A1 | Document Number: Jedi15"/17" WHL-U | Rev: A00

Date: Tuesday, January 08, 2019 | Sheet 85 of 106

Main Func = dGPU





Wistron Corporation

DISCRETE VGA POWER

Jedi15"/17" WHL-U

<Core Design>

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Title
GPU (RSVD)

Size	Document Number	Rev
A3	Jedi15"/17" WHL-U	A00

Date: Tuesday, January 08, 2019 Sheet 87 of 106

<Core Design>

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Title

UNUSED PARTS_(RSVD)

Size	Document Number	Rev
A	Jedi15"/17" WHL-U	A00

Date: Tuesday, January 08, 2019 Sheet 88 of 106

Main Func = UnusedParts

H1 HOLE276R150-GP — ZZ.00PAD.H91
H2 HOLE276R150-GP — ZZ.00PAD.H91
H3 HOLE276R150-GP — ZZ.00PAD.H91
H4 HOLE233R142-GP-U1 — ZZ.00PAD.5S1
H5 HOLE233R142-GP-U1 — ZZ.00PAD.5S1
H6 HOLE233R142-GP-U1 — ZZ.00PAD.5S1
H7 HOLE233R142-GP-U1 — ZZ.00PAD.5S1

WLAN

HS1 STF236R128H128-1-GP — 34.4LO45.001

EMI STOP

SPR1 SPRING-12-GP-U1 — 34.41Y19.001
SPR2 SPRING-12-GP-U1 — 34.41Y19.001

H8 HOLE335R178-GP — ZZ.00PAD.7F1
H9 HOLET375B375X375R174-GP — ZZ.00PAD.XQ1
SB 0911

3D3V_S0
5V_S0
+SDC_IN
5V_S5
3D3V_S5
DCBATOUT
1D2V_S3
BT+

SB 1003 EMC

SSID = EMI

Mind the voltage rating of the caps.

SSID = RF

Layout Placement Request

RF request 2018/09/28 modify

For GPU

Mind the voltage rating of the caps.

Layout Placement Request

RF request 2018/09/28 modify

Jedi UMA/DIS 2IN1

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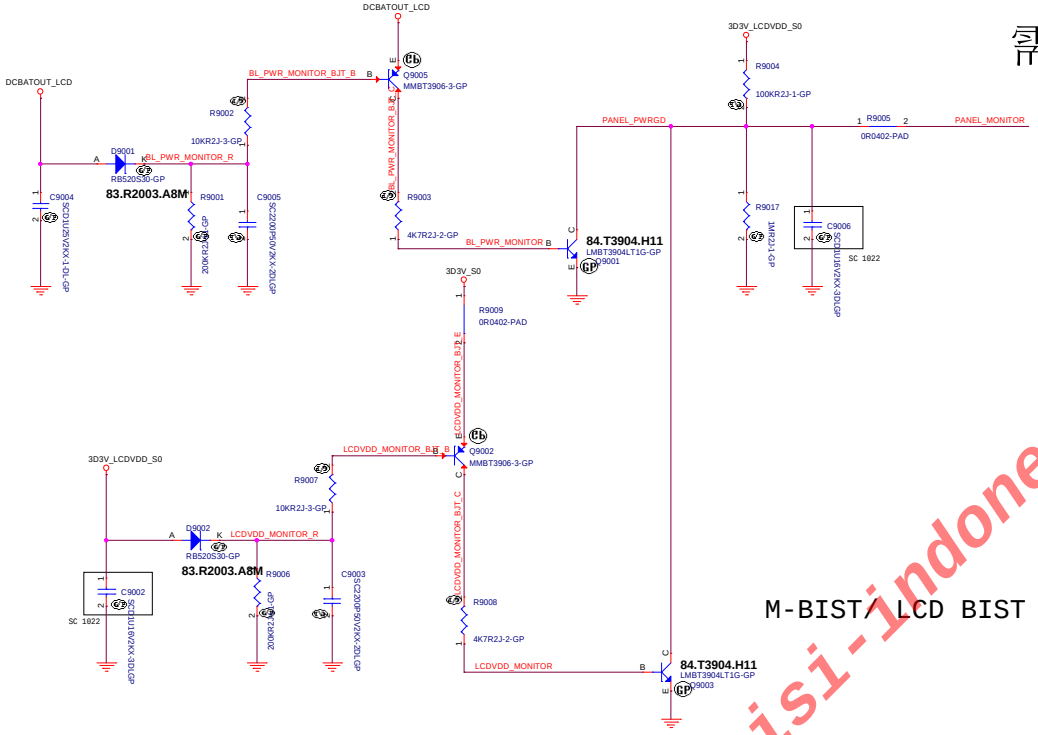
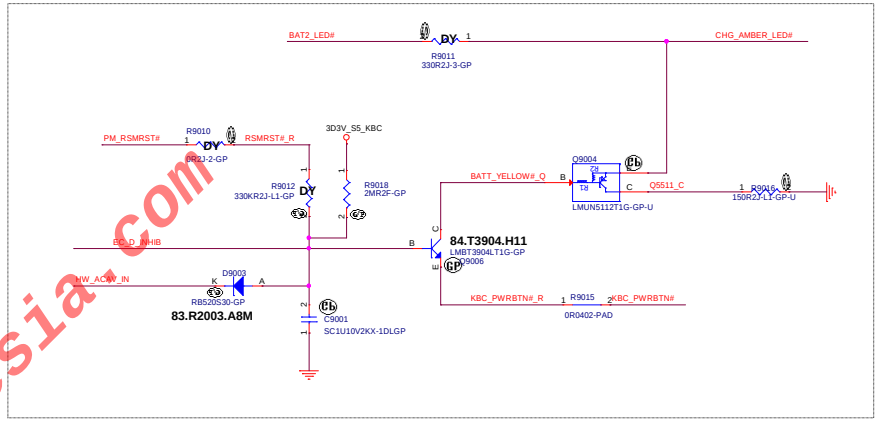
Title: UNUSED PARTS (RF/EMI Caps)
Size: A2 | Document Number: Jedi15"/17" WHL-U | Rev: A00
Date: Tuesday, January 08, 2019 | Sheet 89 of 106

LCD BIST for G10 (Was test only for G9)



需確認 **M-BIST for G10 (Proposed schematic)**



M-BIST/ LCD BIST -1890201

<Core Design>

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Title: M-BIST

Size	Document Number	Rev
A2	Jedi15"/17" WHL-U	A00

Date: Tuesday, January 08, 2019 Sheet 90 of 106

Main Func = TPM

18,25 SPI_SO_ROM
18,25 SPI_CLK_ROM
15,18,25 SPI_SI_ROM
18 SPI_CS_ROM_N2
17,26,61,63,66,76 PLTRST#_CPU
17,24,40 PM_SLP_S0#
20 PIRQA#
18 TPM_SPI_IRQ#

3D3V_S5 R9149 D01R2J-L-GP ST_TPM 3D3V_TPM
3D3V_S0 R9150 D01R2J-L-GP NUVOTON_TPM

3D3V_TPM C9112 C9113 C9109 SCD1U16V2KX-3DLGP SC10U6D3V3MX-DL-GP Pin27 TPM

3D3V_S5_PCH R9148 10KR2J-3-GP NUVOTON_TPM SPI_CS2#_IC

3D3V_TPM R9151 10KR2J-3-GP TPM
R9124 DY 0R2J-2-GP TPM_SPI_IRQ#
SPI_IRQ#_TPM2 R9123 0R2J-2-GP PIRQA#

3D3V_TPM 45mA U9101
SPI_CLK_ROM R9138 33R2J-2-GP TPM
SPI_CS_ROM_N2 R9130 0R2J-2-GP TPM
SPI_SI_ROM R9133 33R2J-2-GP TPM
SPI_SO_ROM R9132 33R2J-2-GP TPM
TP9101 ST_PP
TP9103 ST_GPIO
3D3V_S5 C9106 SC10U6D3V3MX-DL-GP NUVOTON_TPM C9108 SCD1U16V2KX-3DLGP NUVOTON_TPM
TPAD14-OP-GP TP9104 NUVOTON_PP
3D3V_S0 C9104 SCD1U16V2KX-3DLGP NUVOTON_TPM

U9101 ST33HTPH2032AAF3-GP
VPS SPI_RST# SPI_PIRQ# SPI_CLK SPI_CS# MOSI MISO PP GPIO NIC#1 NIC#3 NIC#4 NIC#5 NIC#8 GND
PLTRST#_CPU SPI_IRQ#_TPM2 SPI_CLK_ROM_TPM SPI_CS2#_IC SPI_SI_ROM_TPM SPI_SO_ROM_TPM
NIC#9 NIC#10 NIC#11 NIC#12 NIC#13 NIC#14 NIC#15 NIC#16 NIC#23 NIC#25 NIC#26 NIC#27 NIC#28 NIC#29 NIC#30 NIC#31 NIC#32 NIC#33
TPM_GPIO4 R9118 2K2R2F-GP SPI_CS_ROM_N2
TPM_GPIO0 R9121 DY 0R2J-2-GP PM_SLP_S0#
TPM_GPIO1 TP9102 TPAD14-OP-GP
U9101_2_GND
R9152 0R2J-2-GP ST_TPM

071.33203.0003
Colay
ST33HTPH2032AAF3-GP
071.33203.0003
NPCT750JAAYX-1-GP
071.00750.M001

R9133/R9132/R9138		
CPU TYPE	CNL(16M+8M)	WHL(16M)
Bolt(TPM)	64.33R05.6DL	64.49R95.6DL
Bolt_L (non TPM)	DY	DY

<Core Design>

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Title: TPM2.0
Size: Custom | Document Number: BOLT WHL | Rev: A00
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Jedi UMA/DIS 2IN1

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Title: *Finger Print*

Size	Document Number	Rev
A3	*Jedi15"/17" WHL-U*	*A00*

Date: Tuesday, January 08, 2019 Sheet 92 of 106

(Blanking)

Jedi UMA/DIS 2IN1

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Title: *(Reserved)*

Size	Document Number	Rev
A3	*Jedi15"/17" WHL-U*	*A00*

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(Blanking)

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Title: *(Reserved)*

Size	Document Number	Rev
A3	*Jedi15"/17" WHL-U*	*A00*

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Title: *(Reserved)*

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A3	*Jedi15"/17" WHL-U*	*A00*

Date: Tuesday, January 08, 2019 Sheet 95 of 106

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Title: *(Reserved)*

Size	Document Number	Rev
A3	*Jedi15"/17" WHL-U*	*A00*

Date: Tuesday, January 08, 2019 Sheet 96 of 106

(Blanking)

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Title: *LVDS_Switch*

Size	Document Number	Rev
A3	Jedi15"/17" WHL-U	A00

Date: Tuesday, January 08, 2019 Sheet 97 of 106

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Jedi UMA/DIS 2IN1

Wistron Corporation
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Title: *CRT_Switch*

Size	Document Number	Rev
A3	Jedi15"/17" WHL-U	A00

Date: Tuesday, January 08, 2019 Sheet 98 of 106

Main Func = Debug (MIPI)

<Core Design>

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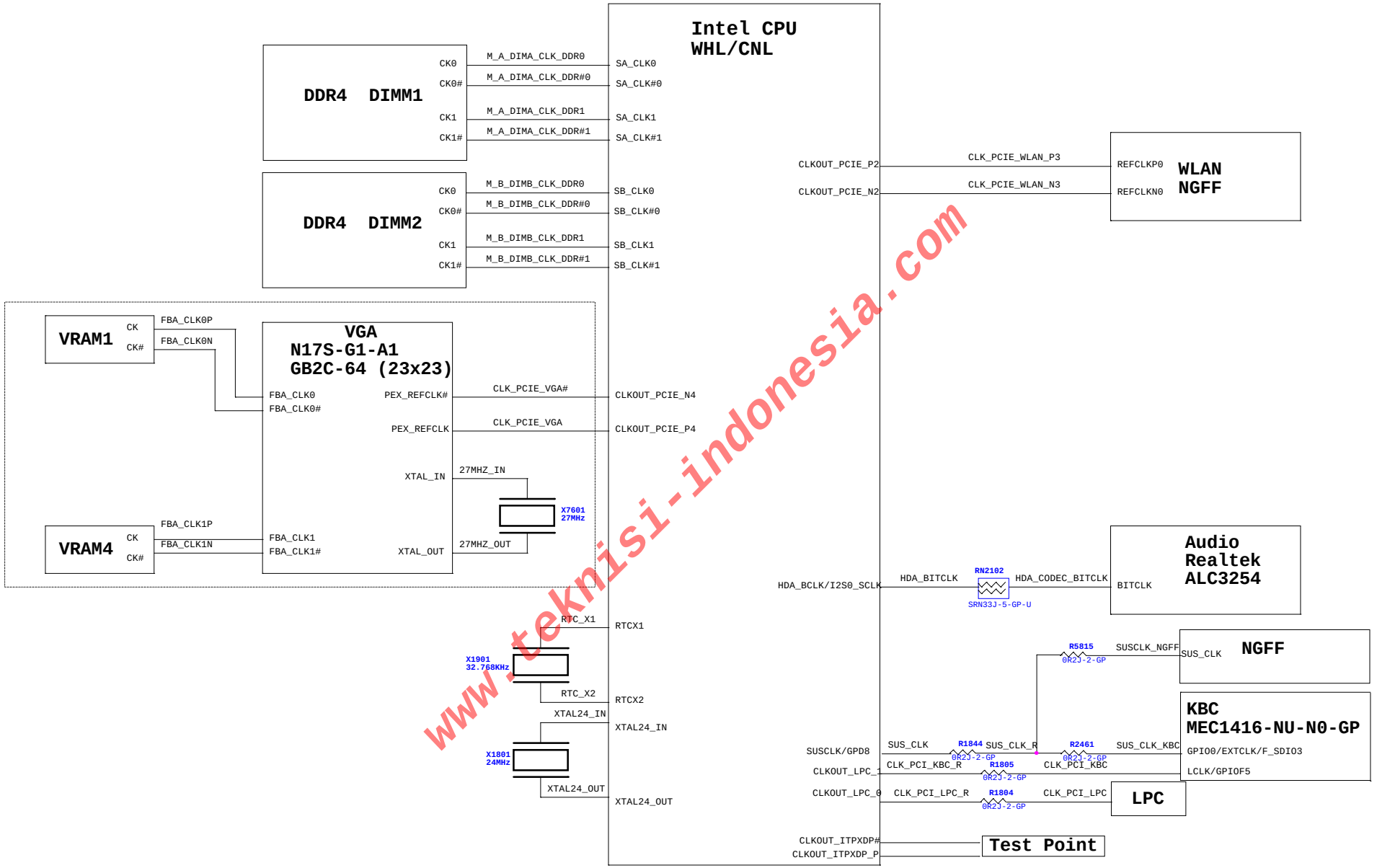
Title: Debug (XDP debug)

Size: A2 | Document Number: Bandon / NorthBay 13" | Rev: A00

Date: Tuesday, January 08, 2019 | Sheet 99 of 106

CLK Block Diagram



Jedi UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CLK Block Diagram

Size: A2 | Document Number: Jedi15"/17" WHL-U | Rev: A00

Date: Tuesday, January 08, 2019 | Sheet 100 of 106

Change notes -

DATE	VERSON	DATE	Page	Modify List	OWNER

Jedi UMA/DIS 2IN1

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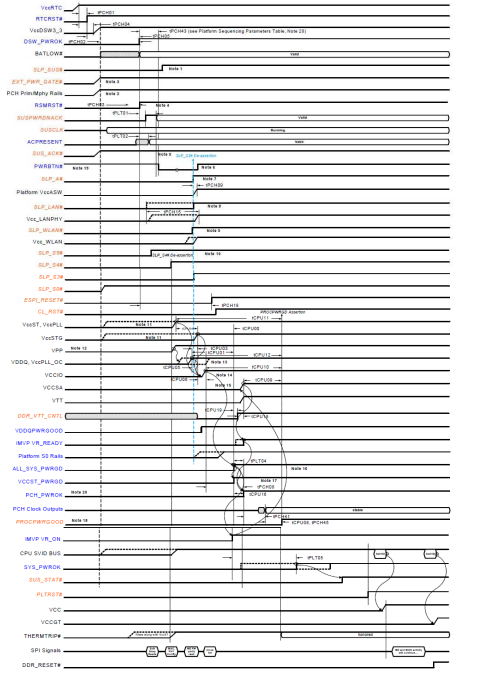
Title: Change History

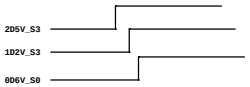
Size	Document Number	Rev
A3	Jedi15"/17" WHL-U	A00

Date: Tuesday, January 08, 2019 Sheet 101 of 106

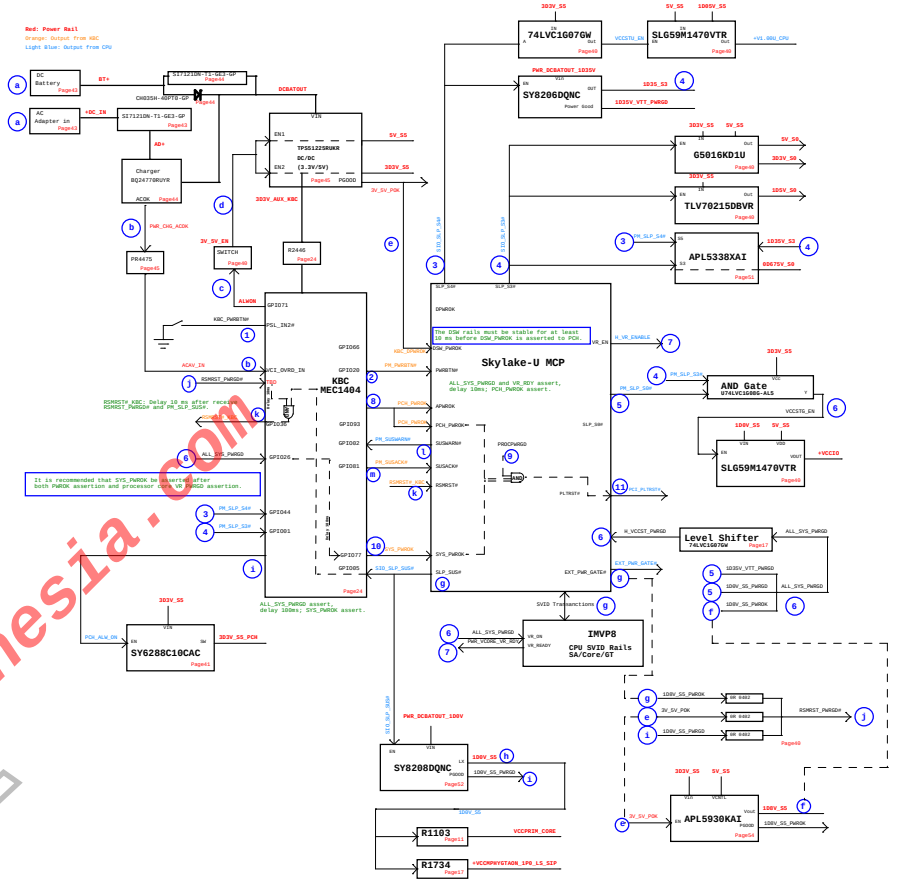
SKL-U/Y Timing Diagram for G3 to S0/M0 [Non Deep Sx Platform]



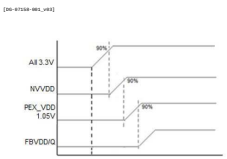
For DDR4 power sequence



Tulip Skylake POWER UP SEQUENCE DIAGRAM (Deep Sx Platform)



[dGPU] N16x Power-Up/Down Sequence



Notes: - All 3.3V includes all rails powered at 3.3V
- PEX_VDD 1.05V includes all rails that are shared

Note:
- The ramp time for any rail must be more than 40 us and is recommended to be less than 2ms.
- The ramp up overshoot should not exceed the silicon reliability limit voltage.
- The previous power rail must ramp up to 90% before the next power rail can start ramping up.
- No signal should be applied to the GPU before the power rails are fully ramped
- Refer to the JEDEC Memory Specification for memory related power sequencing.
- The order of NVVDD and PEX_VDD ramp-up can be reversed during GC6 exit when there is a back-to-back GC6 entry/exit and/or when PEX_VDD takes longer to ramp down during GC6 entry.

3.10.2.2 Power-Down Sequence

There is no specific power down sequence. However, residual voltage from power down must not violate the power-up sequence when back to back GPU power-down and power-up events take place.

18.3.2.3 GC6 2.0 Entry/Exit Timing

The following timing diagram in Figure 18-12 and Table 18-3 describes the GC6 2.0 en and exit sequence and timing requirements.

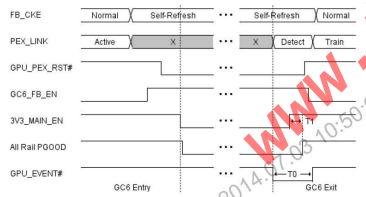
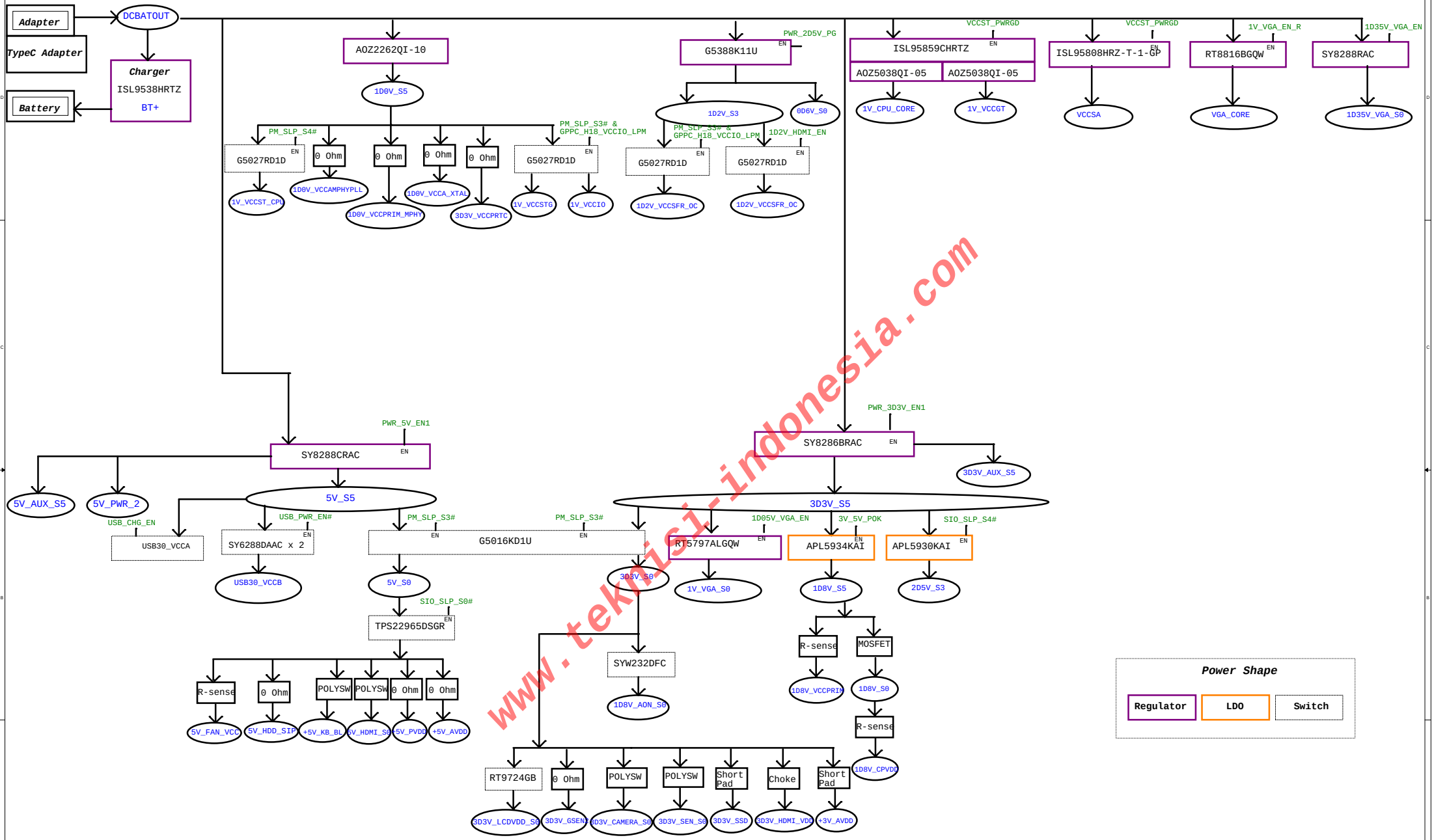


Figure 18-12. GC6 2.0 Entry/Exit Sequence Timing Diagram

Table 18-2. GC6 2.0 Entry/Exit Sequence Timing Parameters

Symbol	Description	Min	Max	Unit
T0	GPU_EVENT# assertion period	0.001	N/A	ms
T1	3V3_MAIN_EN assertion to all power rails up and stable	0.04	4	ms

Note:
- ALL Rail PGOOD=1 represents all GPU power rails are ramped up and in regulation. If any GPU power rail cannot be guaranteed in regulation this state should equal to 0.
- During GC6 exit, the order of power rail ramp-up must follow the power-up sequence described in Chapter 3 with the exception that FBVDD/Q stays on.
- All delays should be minimized to increase time spent in GC6 for maximum power saving.
- The entire entry/exit sequence must complete within 200 ms.



<Core Design>

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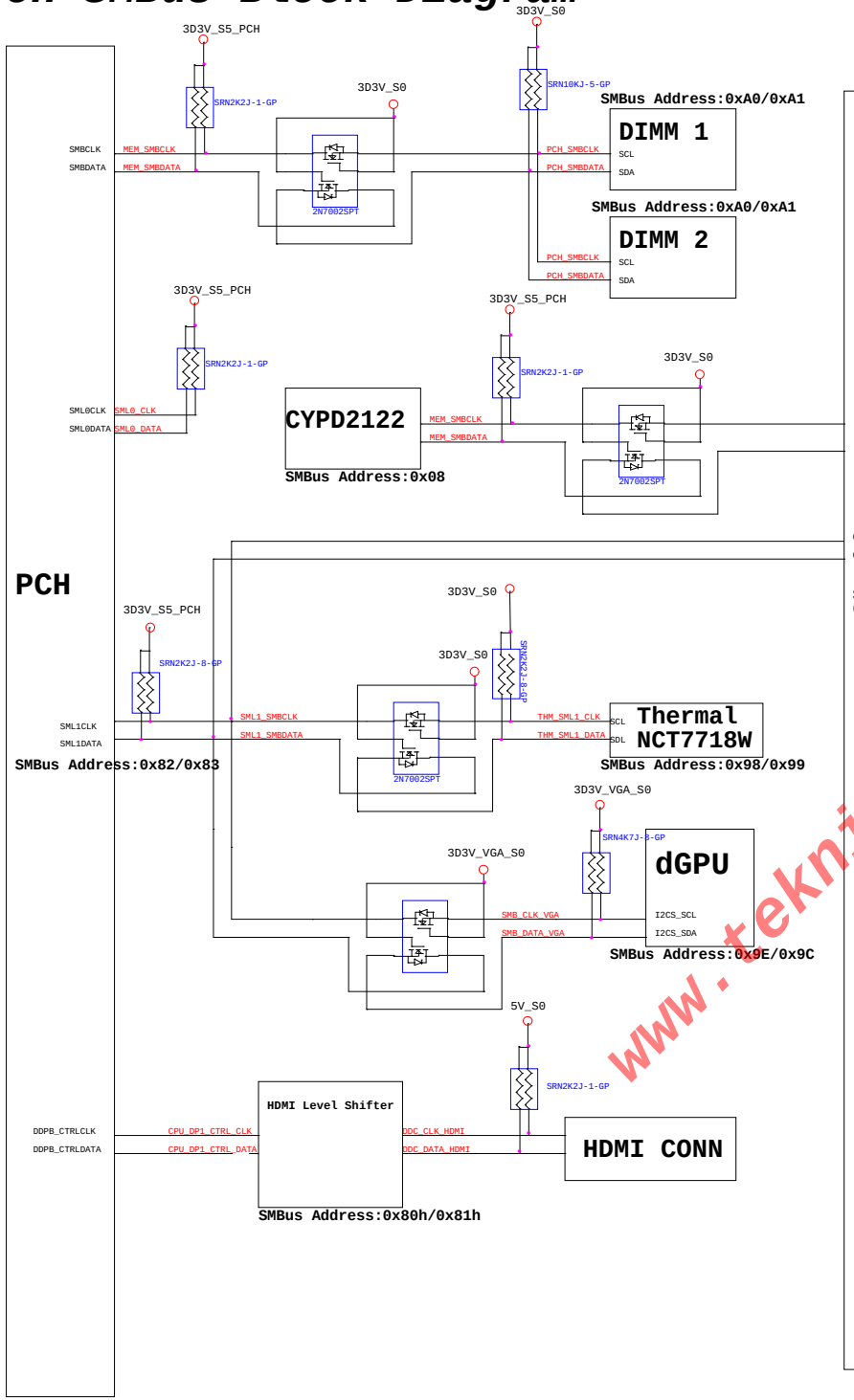
Title: Power Block Diagram

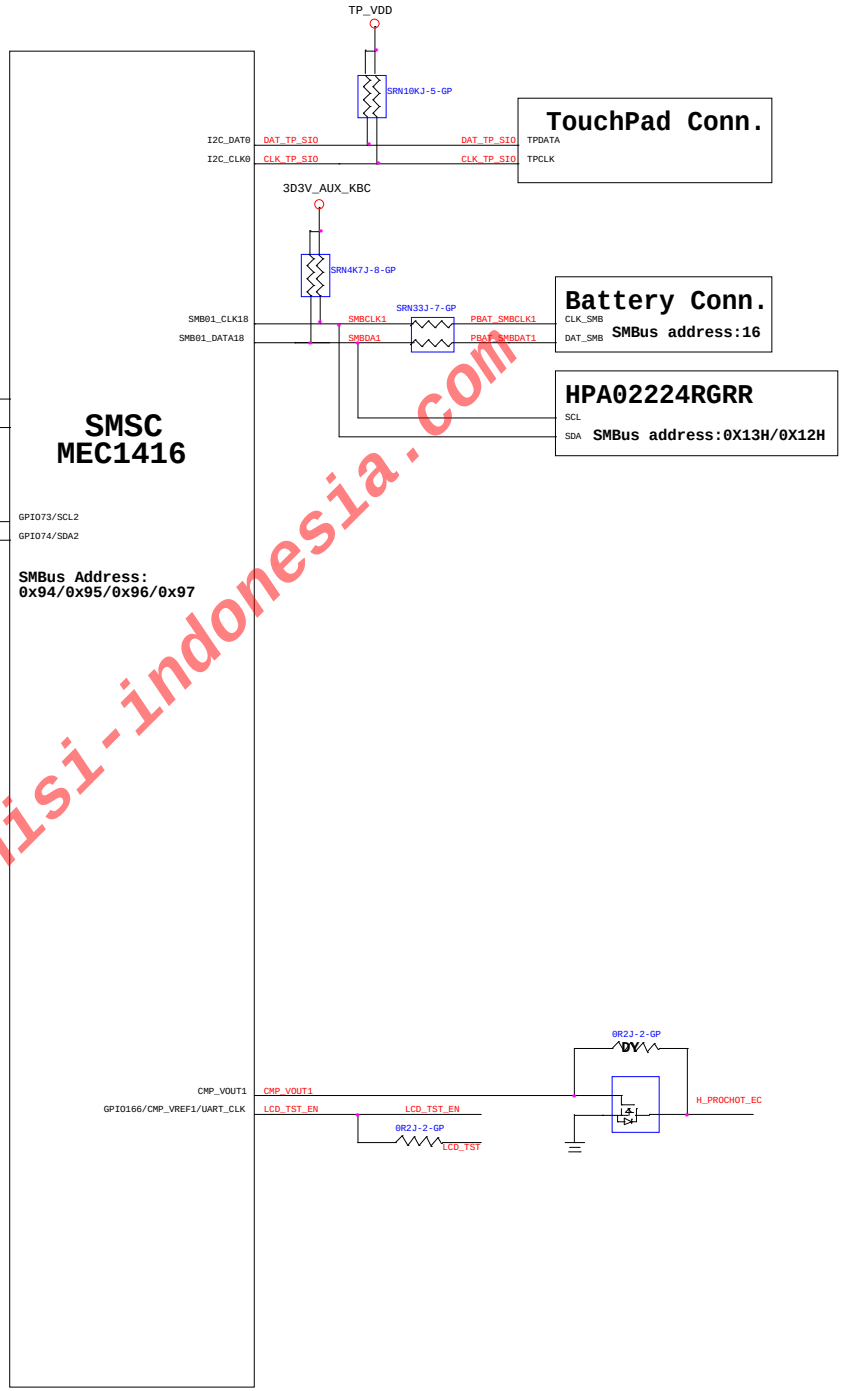
Size: A2 | Document Number: Jedi15"/17" WHL-U | Rev: A00

Date: Tuesday, January 08, 2019 | Sheet 103 of 106

PCH SMBus Block Diagram



KBC SMBus Block Diagram



Jedi UMA/DIS 2IN1

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Title: SMBUS Block Diagram

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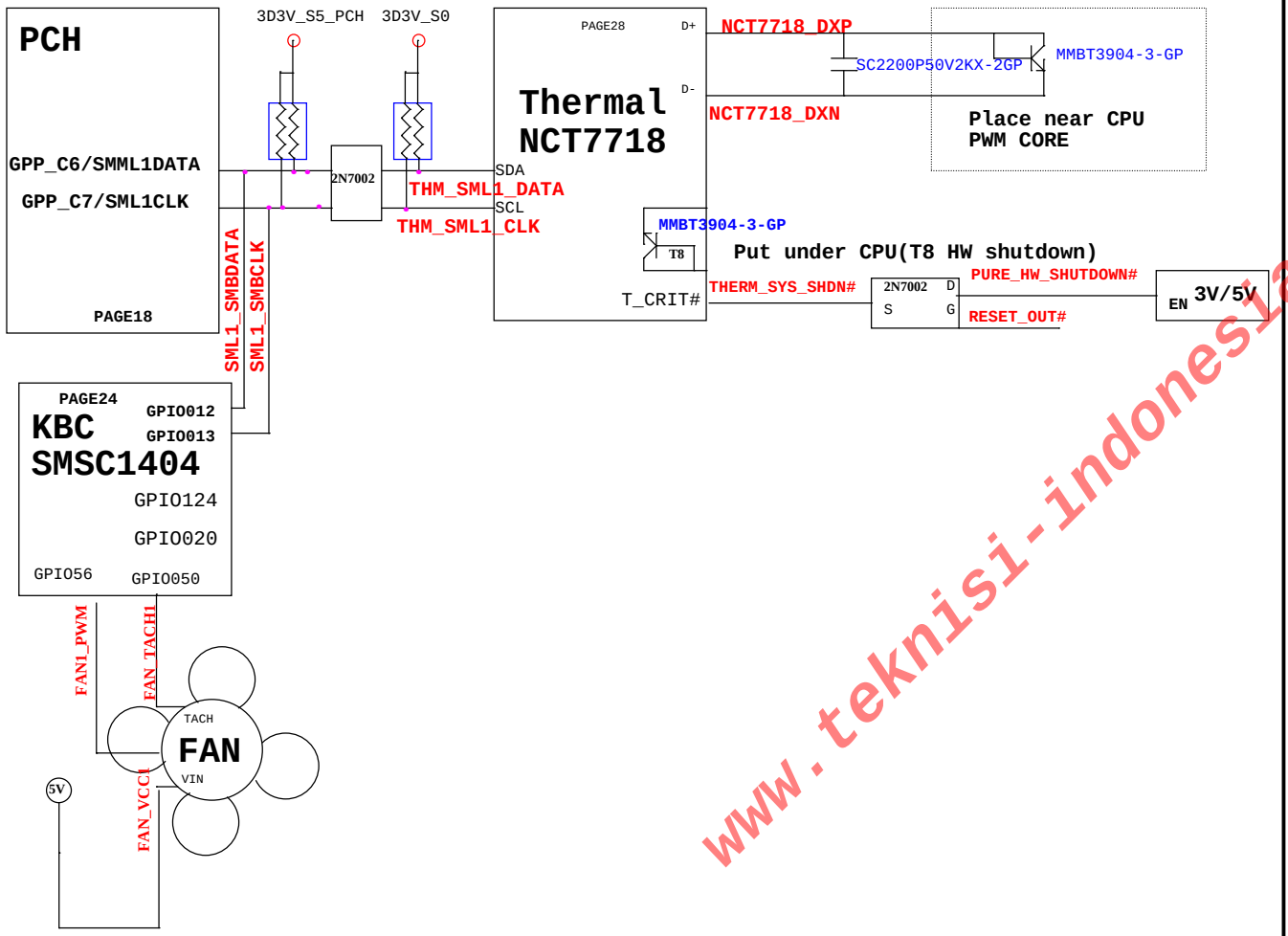
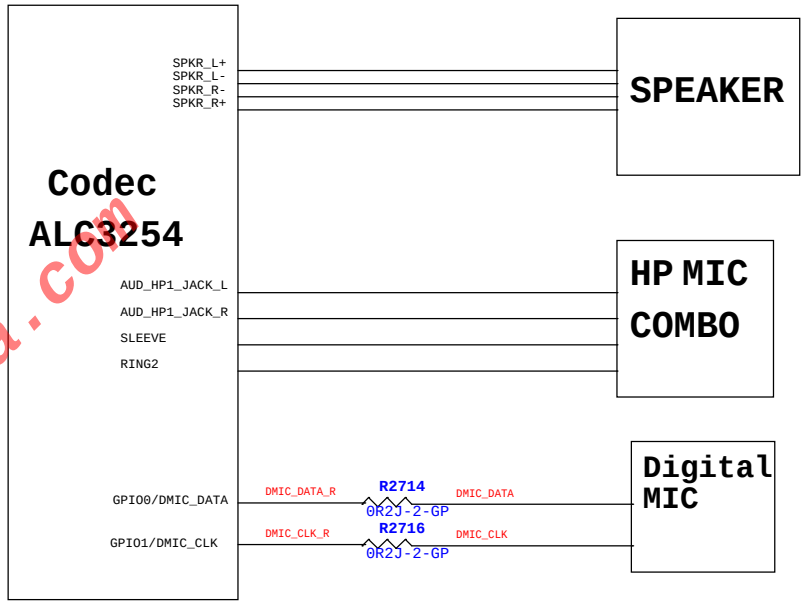
A2	Jedi15"/17" WHL-U	A00

Date: Tuesday, January 08, 2019 Sheet 104 of 106

Thermal Block Diagram



Audio Block Diagram



Jedi UMA/DIS 2IN1

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Title: Thermal/Audio Block Diagram

Size: Custom | Document Number: Jedi15"/17" WHL-U | Rev: A00

Date: Tuesday, January 08, 2019 | Sheet 105 of 106

Jedi UMA/DIS 2IN1

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Title

SIP connector

Size	Document Number	Rev
A	***Jedi15"/17" WHL-U***	***A00***

Date: Tuesday, January 08, 2019 Sheet 106 of 106